EPSON

SED1353

STN Color LCD Controller

- Color/monochrome LCD controller
- Pin convertible with SED1352 (monochrome LCD controller)
- Low operating voltage (2.7V to 5.5V)
- Supports interface with various types of MPUs

■ DESCRIPTION

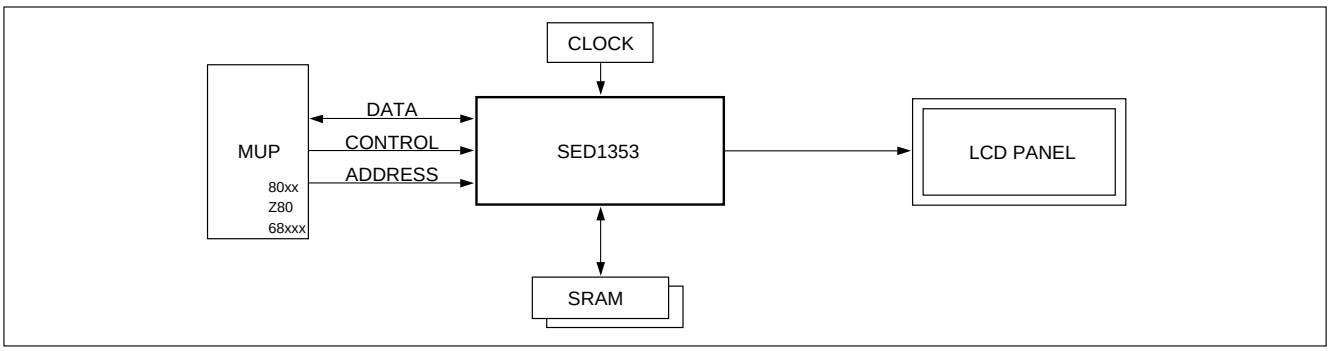
SED1353 is a dot matrix graphics LCD controller capable of supporting up to 1024 × 1024 (monochrome display) resolution. 256-color-display out of 4096 colors and monochrome display in up to 16-level gray scale display are available. SED1353 allows easy connection with MC68000 families and other 8/16 bits MPUs. As for memory for the display, it supports up to 128 KB SRAM.

Low operating power of SED1353 makes it a most suitable color LCD controller not only for factory automation equipments but also for small hand held equipments, too.

■ FUNCTIONS

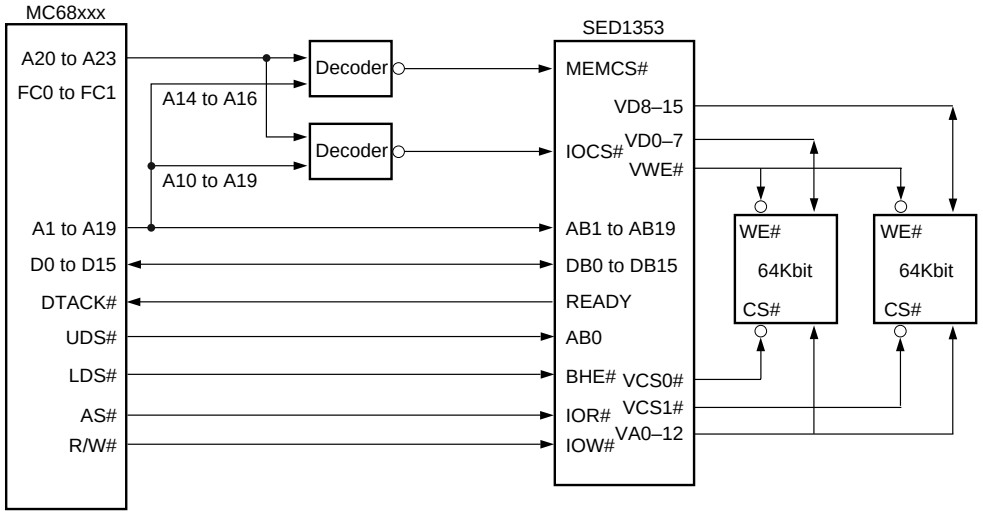
- 16-bit, 16 MHz and MC68xxx MPU interface.
- READY or WAIT# terminal controlled 8/16 bits MPU interface.
- Either index register approah or direct mapping can be selected when making access to the internal register.
- Support a crystal oscillator or external clock input.
- 8/16 bits SRAM interface.
- Designed to operate at low power.
- Designed for two types of power save mode.
- Setup of virtual display sreen is available.
- Supports split-screen (displays two different pages on a single screen).
- Display mode:
  Black and white binary display.
  2/4 bits per pixel, 4/16-levelgray-scale-display.
  2/4/8 bits per pixel, 4/16/256-level-gray-scale-display.
- Display memory interface
  128KB (one 64K × 16 SRAM)
  128KB (two 64K × 8 SRAM)
  64KB (two 32KB × 8 SRAM)
  40KB (8K x 8 SRAM and 32K × 8 SRAM)
  32KB (one 32K × 8 SRAM)
  16KB (two 8K × 8 SRAM)
  8KB (one 8K × 8 SRAM)
- LCD panel supported:
  Single screen drive STN panel
  Dual screen drive STN panel
- Maximum number of vertical lines:
  1024 lines (for single screen drive)
  2048 lines (for dual screen drive)
- SED1353D0A: Chip shipped.
- SED1353F0A: QFP5-100 pin
- SED1353F1A: QFP15-100 pin

■ SYSTEM CONFIGURATION DIAGRAM



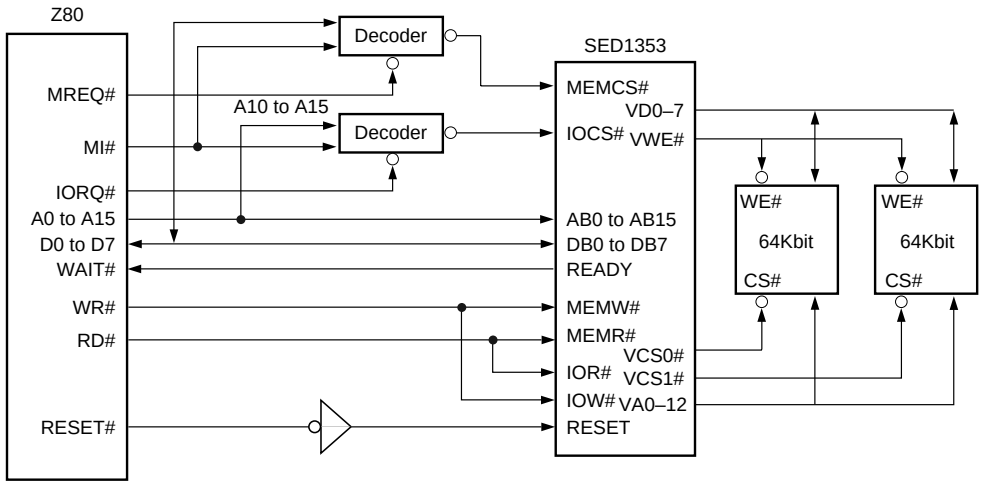
■ SYSTEM INTERFACE

16-bit MC68xxx MPU & 16KB SRAM (2 of 8K × 8)



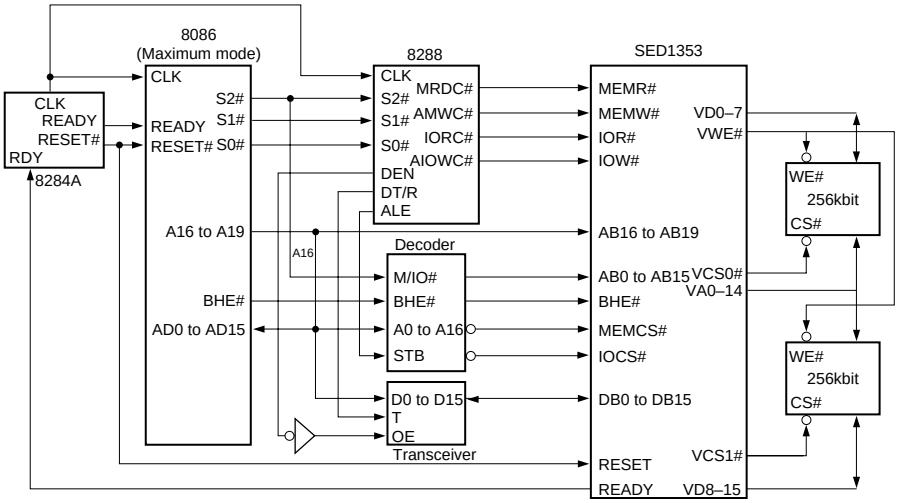
Note: Example implemation, actual may vary

8-bit Z80 MPU & 16KB SRAM (2 of 8K × 8)



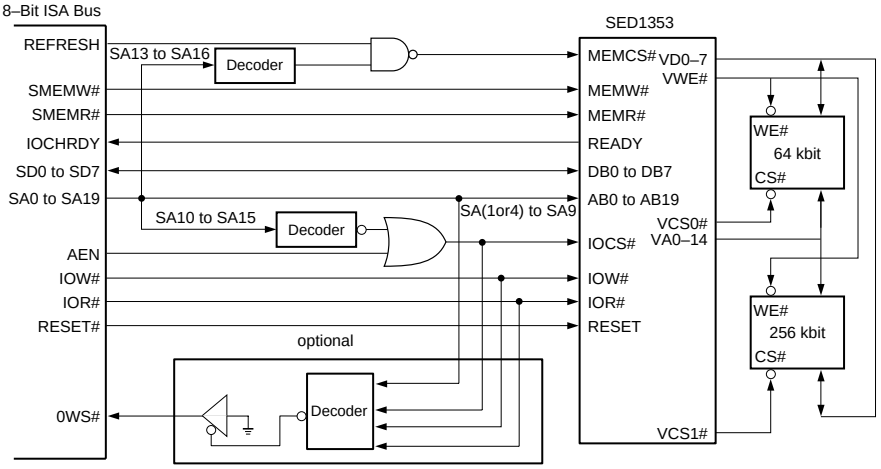
Note: Example implemation, actual may vary

16-bit 8086 MPU & 64KB SRAM (2 of 32K × 8)



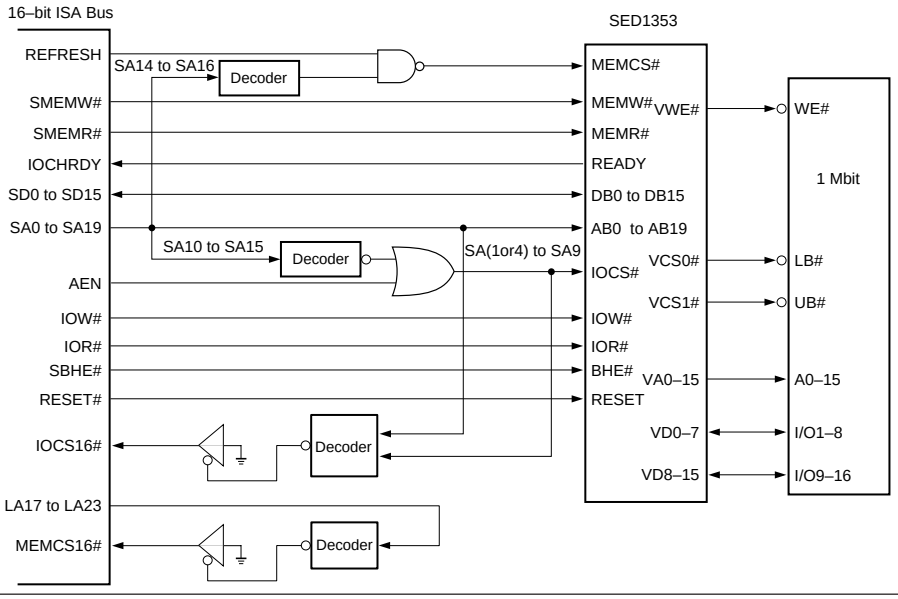
Note: Example implemation, actual may vary

8-bit ISA Bus & 40KB SRAM (1 of 8K × 8 & 1 of 32K × 8)



Note: Example implemation, actual may vary

16-bit ISA Bus & 128KB SRAM (1 of 128K × 8)



Note: Example implemation, actual may vary

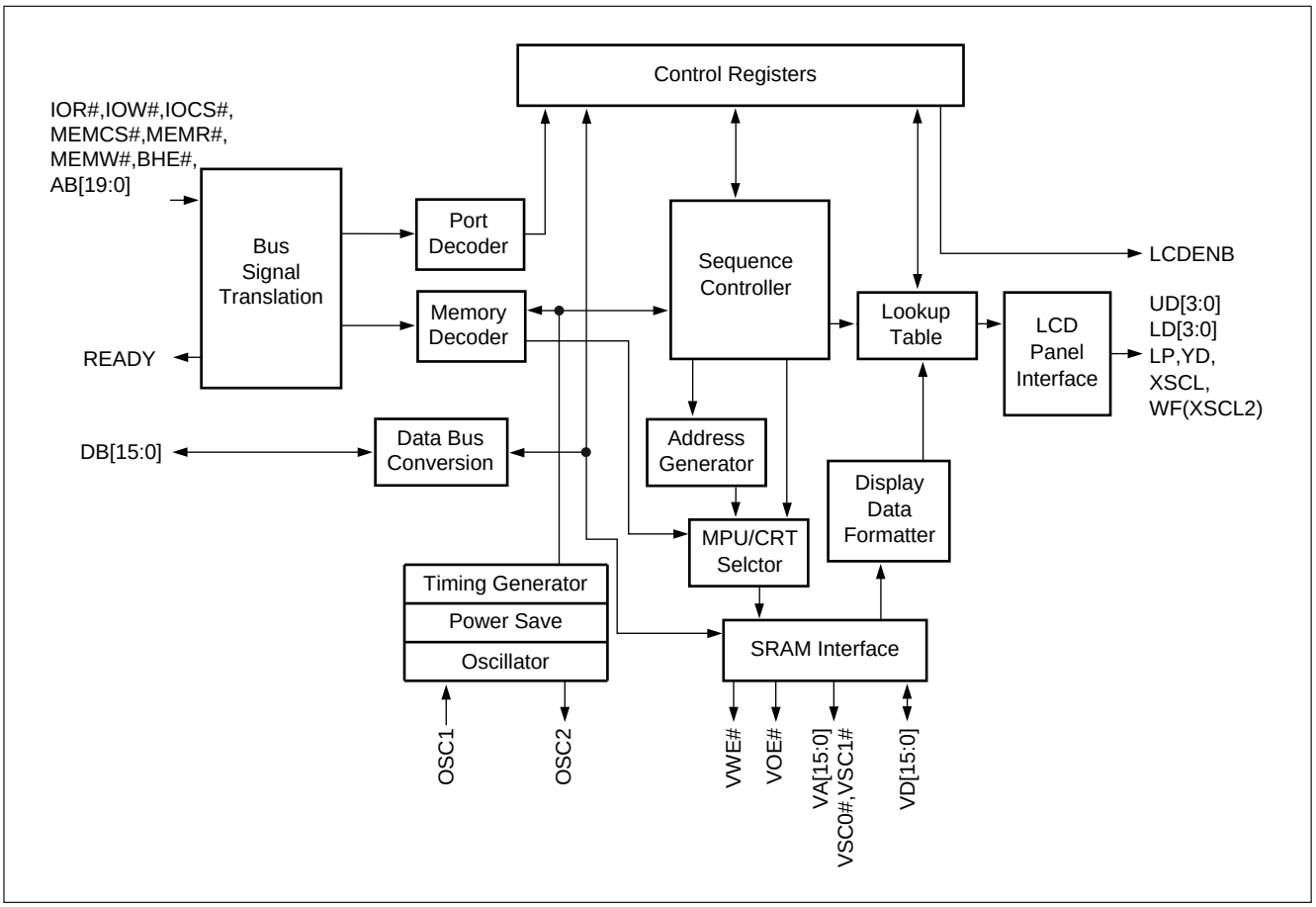
■ RESOLUTIONS SUPPORTED

Display RAM	Example Display Size				SRAM Type	CPU Interface	SRAM Interface
	Monochrome	4 Grays/ Colors	16 Grays/ Colors	256 Colors*			
	X Y	X Y	X Y	X Y			
8KB	320 × 200	256 × 128	128 × 128	—	1 of 8K × 8	8-bit	8-bit
16KB	512 × 256	320 × 200	200 × 160	160 × 100*	2 of 8K × 8	8-bit	8-bit/16-bit
						16-bit	16-bit
32KB	512 × 512	512 × 256	256 × 256	192 × 100*	1 of 32K × 8	8-bit	8-bit
40KB	1024 × 320	512 × 320	320 × 256	320 × 128*	1 of 8K × 8 & 1 of 32K × 8	8-bit	8-bit
64KB	1024 × 512	512 × 512	512 × 256	256 × 256*	2 of 32K × 8	8-bit	8-bit/16-bit
						16-bit	16-bit
128KB	1024 × 1024	1024 × 512	512 × 512	512 × 256*	1 of 64K × 16	16-bit	16-bit
					2 of 64K × 8	16-bit	16-bit

Note: * 256 colors must use 16-bit SRAM interface

The above display sizes depend on number of gray scale (colors) and memory capacity.

■ BLOCK DIAGRAM



■ OVERVIEW OF THE FUNCTIONAL BLOCKS

BUS Signal Translation

This block converts the SED1353 internal bus so that it may be used for MC68000 series MPU or READY terminal controlled MPU series. This conversion is done through the setting of VD2 terminal from the Configuration Option (see page 11).

Control Register

This register block consists of 16 types of control registers. Access to these registers are available either through the direct mapping approach or index register approach.

Sequence Controller

This block generates horizontal and vertical display timing being set up in the internal register.

LCD Panel Interface

This block selects a gray scale for passive monochrome and color LCD panels through timing, then outputs data to the LCD panel.

Lookup Table

This block consists of each RGB 16 × 4-bit palettes. In the monochrome gray scale mode, a gray scale pattern can be specified using the "Green" palette. In the color mode, all RGB palettes are used to set up a color pattern out of 4096 colors.

Port Decoder

This decoder validates a given I/O cycle through setup of VD1 terminal, VD2 to VD4 terminals, IOCS # terminal and address lines AB9 to 1 from the Configuration Option (see page 11).

Memory Decoder

This decoder validates a given memory cycle through setup of VD15 to VD13, MEMCS # terminal and address lines AB19 to 17 from the Configuration Option (see page 11).

Data Bus Conversion

This block connects an external data bus (8 or 16 bits) to the internal data bus through the setup of V_{DD} terminal from the Configuration Option (see page 11).

Address Generator

This block generates the address used to validate access to the display memory.

MPU/CRT Selector

This block arbitrates between MPU accees to the display memory and an access to it for LCD display.

Display Data Fomatter

This block reads data from the display memory, then outputs it in the format consistant with the specified display mode (monochrome/color, levels of gray scale and number of colors).

Clock Inputs/Timing

This block generates a master clock (mclk) conforming to the specified gray scale leves 1, number of colors and display memory interface. The following master clocks are available depeding on conditions specified:

– mclk = input clock: 16-grays/16-color mode (8-bit display memory) or 256-color mode (16-bit display memory).
– mclk = 1/2 input clock: B&W, 4-grays/4-color mode (8-bit display memory), or 16-grays scale/16-color mode (16-bit display memory).
– mclk = 1/4 input clck: B&W, 4-grays scale/4-color mode (16-bit display memory).

Pixel clock = input clock = f_{OSC}

SRAM Interface

This block generates the interface signal to the display memory (SRAM).

■ DC CHARACTERISTICS

● Absolute Maximum Ratubgs

Item	Code	Rating	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3 + 6.0	V
Input voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.5	V
Output voltage	V_{OUT}	V_{SS} – 0.3 to V_{DD} + 0.5	V
Storage voltage	T_{STG}	–65 to 150	°C

● Recommended Operation Conditions

Item	Code	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	V_{SS} = 0 V	2.7	3.0/3.3/5.0	5.5	V
Input voltage	V_{IN}		V_{SS}	—	V_{DD}	V
Operating current	I_{OPR}	f_{OSC} = 6MHz, 256 colors		4.5/5.0/11		mA
Operating voltage	T_{OPR}		–40	25	85	°C

● Input Characteristics

Item	Code	Conditions	Min	Typ	Max	Unit
Low level input voltage	V_{IL}	V_{DD} = 4.5V V_{DD} = 3.0V V_{DD} = 2.7V			0.8 0.4 0.3	V
High level input voltage	V_{IH}	V_{DD} = 5.5V V_{DD} = 3.6V V_{DD} = 3.3V	2.0 1.3 1.2			V
Positive threshold	V_{T+}	V_{DD} = 5.0V V_{DD} = 3.3V V_{DD} = 3.0V			2.4 1.4 1.3	V
Negative threshold	V_{T-}	V_{DD} = 5.0V V_{DD} = 3.3V V_{DD} = 3.0V	0.6 0.5 0.4			V
Hysteresis voltage	V_H	V_{DD} = 5.0V V_{DD} = 3.3V V_{DD} = 3.0V	0.1 0.1 0.1			V
Leak voltage	I_{IZ}	—	–1		1	µA
Input pin capacity	C_{IN}	f = 1MHz, V_{DD} = 0V			12	pF
Pulldown resistance	R_{PD}	V_{DD} = 5.0V, V_I = V_{DD}	50	100	200	kΩ
Pulldown resistance	R_{PD}	V_{DD} = 3.3V, V_I = V_{DD}	90	180	360	kΩ
Pulldown resistance	R_{PD}	V_{DD} = 3.0V, V_I = V_{DD}	100	200	400	kΩ

● Output Characteristics

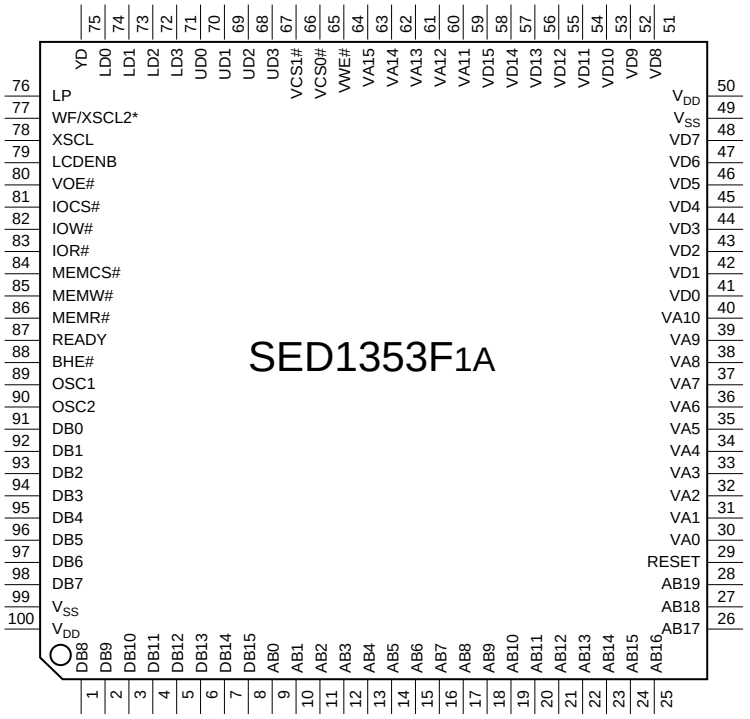
Item	Code	Conditions	Min	Typ	Max	Unit
Low level output voltage Type 1: TS1D2, CO1 Type 2: TS2 Type 3: TS3, CO3, CO3S	V_{OL} (5.0V)	V_{DD} = Min I_{OL} = 4mA I_{OL} = 8mA I_{OL} = 12mA			0.4	V
Low level output Type 1: TS1D2, CO1 Type 2: TS2 Type 3: TS3, CO3, CO3S	V_{OL} (3.3V)	V_{DD} = Min I_{OL} = 2mA I_{OL} = 4mA I_{OL} = 6mA			0.3	V
Low level output voltage Type 1: TS1D2, CO1 Type 2: TS2 Type 3: TS3, CO3, CO3S	V_{OL} (3.0V)	V_{DD} = Min I_{OL} = 1.8mA I_{OL} = 3.5mA I_{OL} = 5mA			0.3	V
High level output voltage Type 1: TS1D2, CO1 Type 2: TS2 Type 3: TS3, CO3, CO3S	V_{OH} (5.0V)	V_{DD} = Min I_{OL} = –4mA I_{OL} = –8mA I_{OL} = –12mA	V_{DD} – 0.4			V
High level output voltage Type 1: TS1D2, CO1 Type 2: TS2 Type 3: TS3, CO3, CO3S	V_{OH} (3.3V)	V_{DD} = Min I_{OL} = –2mA I_{OL} = –4mA I_{OL} = –6mA	V_{DD} – 0.3			V
High level output voltage Type 1: TS1D2, CO1 Type 2: TS2 Type 3: TS3, CO3, CO3S	V_{OH} (3.0V)	V_{DD} = Min I_{OL} = –1.8mA I_{OL} = –3.5mA I_{OL} = –5mA	V_{DD} – 0.3			V
Output leak current	I_{OZ}	—	–1		1	µA
Output pin capacity	C_{OUT}	f = 1MHz, V_{DD} = 0V			12	pF
Bi-directional pin capacity	C_{BID}	f = 1MHz, V_{DD} = 0V			12	pF

■ SED1353F0A PIN LAYOUT

* Pin No.80 = WF: Supports every display mode except for 8-bit single color panel interface (format 1).

* Pin No.80 = XSCL2: Supports 8-bit single color panel interface (format 1).

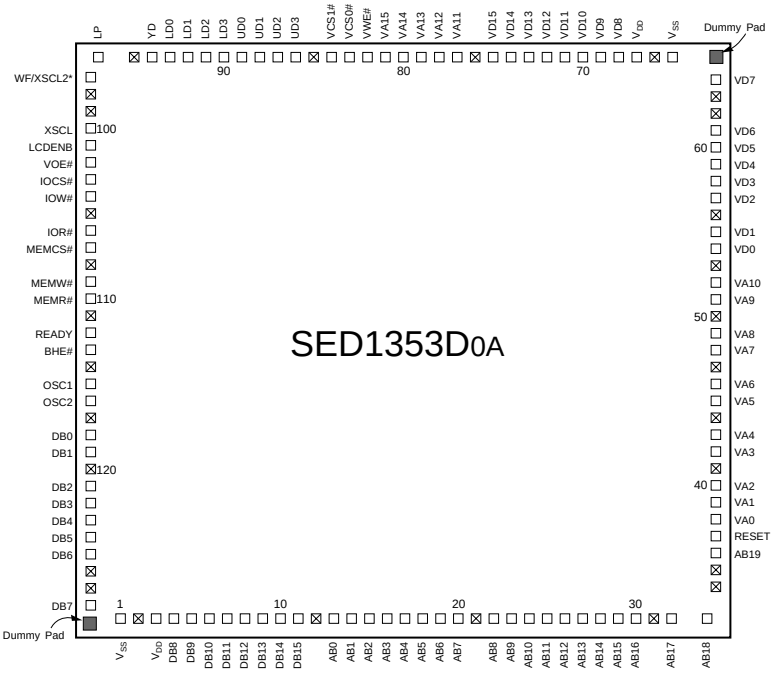
■ SED1353F1A PIN LAYOUT



* Pin No. 77 = WF: Supports every display mode except for 8-bit single color panel interface (format 1).

* Pin No. 77 = XSCL2: Supports 8-bit single color panel interface (format 1).

■ SED1353D0A PIN LAYOUT



Chip Size	=	5.030mm x 5.030mm
Chip Thickness	=	0.400mm
Pad size	=	0.090mm x 0.090mm
Pad Pitch	=	0.126mm (Min.)

* Pad No. 97 = WF: Supports every display mode except for 8-bit single color panel interface (format 1).

* Pad No. 97 = XSCL2: Support 8-bit single color panel interface (format 1).

■ PIN DESCRIPTION

I = Input
O = Output
I/O = Input and output
P = Power supply

● Bus Interface

Pin name	Type	F0A Pin No.	F1A Pin No.	D0A Pin No.	Description
DB0–DB15	I/O	94–100, 1, 4–11	91–98, 1–8	118–119, 121–125, 128, 4–11	Connects to the system data bus. In 8-bit bus mode, DB8 to DB15 connect to VD0.
AB0	I	12	9	13	When MC68000 MPU interface is used, it connects to UDS#pin (Upper Data Strobe). When other bus interface is used, it connect to the system address bus.
AB1–AB19	I	13–31	10–28	14–20, 22–30, 32–33, 36	Connects to the system bus.
BHE#	I	91	88	113	When MC68000 MPU interface is used, it connects to LDS# pin (Lower Data Strobe). When other bus interface is used, this pin functions as the bus high enable input on the 16-bit system. On 8-bit bus system, it connects to VDD.
IOCS#	I	84	81	103	Select one of 15 internal registers.
IOW#	I	85	82	104	When MC68000 MPU interface is used, it connects to R/W# pin. This input pin selects either read cycle (active high) or write cycle (active low) for data transmission. When other bus interface is used, it is active low to write data to the internal register.
IOR#	I	86	83	106	When MC68000 MPU interface is used, it connects to AS# pin. On the address bus, this input pin indicates an valid address is available. When other bus interface is used, this pin is active low and reads data from the internal register.
MEMCS#	I	87	84	107	Accepts active low inputs, it displays access attempts to the display memory.
MEMW#	I	88	85	109	Accepting active low inputs, it writes dat a to the display memory. When MC68000 MPU interface is used, it connects to VDD.
MEMR#	I	89	86	110	Accepting active low inputs, it reads data from the display memory. When MC68000 MPU interface is used , it connects to VDD.
READY	O	90	87	112	When MC68000 MPU interface is used, it is connected with DATCK# pin. As data transfer completes, it is turned low. When other system bus interface is used, it outputs low if the system wait status is needed. As data transfer completes, READY state is reset to return to High-Z.
RESET	I	32	29	37	Accepting active high, it turns all signals non-active.

● Display Memory Interface

Pin name	Type	F0A Pin No.	F1A Pin No.	D0A Pin No.	Description
VD0–VD15	I/O	44–51, 54–61	41–48, 51–58	54–55, 57–61, 64, 68–75	They connect to the display memory data bus. When 16-bit interface is used, VD0 to VD7 are connected to the display memory buses in even byte address, and VD8 to VD15 are connected to those in odd memory address. When RESET is turned to high, output drivers of these pins are set to High-Z. At the falling edge of RESET, values of VD0 to VD15 are latched by this IC allowing to set various hardware options.
VA0–VA15	O	33–43, 62–66	30–40, 59–63	38–40, 42–43, 45–46, 48–49, 51–52, 77–81	They connect to the display memory address buses.
VCS1#	O	69	66	84	It outputs active low chip select signal to the second SRAM or SRAMs at odd byte address.
VCS0#	O	68	65	83	It outputs active low chip select signal to the first SRAM or SRAMs at even byte address.
VWE#	O	67	64	82	It outputs active low used when writing data to the display memory. It is connected to the SRAM WE# pin.
VOE#	O	83	80	102	It outputs active low used for reading data from the display memory. It is connected to the SRAM OE# pin.

● LCD Interface

Pin name	FPDI-1* Pin name	Type	$F0_A$ Pin No.	$F1_A$ Pin No.	$D0_A$ Pin No.	Description
UD3–UD0 LD3–LD0	UD3–UD0 LD3–LD0	O	70–73 74–77	67–70 71–74	86–89 90–93	Display data in the dual panel mode. When 4-bit single panel is employed, LD3 to LD0 are driven to low.
XSCL	FPSHIFT	O	81	78	100	Shift clock of display data. Aft the falling edge of this signal, data is shifted to X driver on the LCD.
LP	FPLINE	O	79	76	96	Latch clock of display data. At the falling edge of this signal, line data on the LCD X driver is latched and used for turning on the LCD Y driver.
WF/XSCL2	MOD FPSHIFT2	O	80	77	97	The second shift clock for 8-bit single color panel (format) mode. In other modes, it becomes LCD back plane bias signal. This output is toggled one time at each frame. (Setup of WF signal output may be changed from the internal register.)
YD	FPFRAME	O	78	75	94	Vertical scan start signal.
LCDENB	—	O	82	79	101	LCD enable signal. Using this signal, you can externally turn off the panel power and back light.

*: Conforming to the VESA flat panel interface standard.

● Clock Input

Pin name	Type	$F0_A$ Pin No.	$F1_A$ Pin No.	$D0_A$ Pin No.	Description
OSC1	I	92	89	115	When 2-pin crystal is used for the clock input, this pin is connected to the crystal along with OSC2. And, when an external oscillator circuit is used as the clock source, this pin inputs the clock.
OSC2	O	93	90	116	When 2-pin crystal is used for the clock input, this pin is connected to the crystal along with OSC2. And, when an external oscillator circuit is used as the clock source, it is turned to NC.

● Power Supply

Pin name	Type	$F0_A$ Pin No.	$F1_A$ Pin No.	$D0_A$ Pin No.	Description
V_{DD}	P	3, 53	50, 100	3, 67	Power supply pin.
V_{SS}	P	2, 52	49, 99	1, 65	Grounding pin.

■ OPTIONAL HARDWARE CONFIGURATION

During the RESET, SED1353 latches state of SRAM data bus (1 or 0) to offer an optimum hardware configuration to the user system. Since SED1353 has a pull down resistor inside the IC, if the following "1" applies, a 10kΩ external pull up resistor must be provided . In case of "0", the external pull up resistor is not required.

Pin name	Hardware configuration according to the pin status (1 or 0)	
	1	0
VD0	16-bit host bus interface	8-bit host bus interface
VD1	Direct mapping I/O access	Index mapping I/O access
VD2	MC68000 MPU interface	READ (WAIT#) pin controlled MPU and bus interface
VD3	When 16-bit bus interface is used, there is data swap between higher-order data byte and lower-order data byte.	When 16-bit bus interface is used, there is not data swap between higher-order and lower-order data byte.
VD12–VD4	I/O mapping address select bit [9:1] Initial bits used for selecting the address mapping of I/O resistor. hey correspond to the address bit [9:1] of MPU interface. When valid address for I/O cycle is generated, the internal decoder is controlled so that addressing is as specified with these bits.	
VD15–VD13	Memory mapping address select bit [3:1] Initial bits used for selecting address mapping of memory. They correspond to address bit [19:17] of the MPU interface. When valid address for memory cycle is generated, the internal decoder is controlled so that addressing is done as specified with these bits. "Valid memory cycle" denotes the the access where MEMCS"# is turned low.	

■ COMPARISON BETWEEN SED1353 AND SED1352

SED1353 is upward convertible and pin convertible with f SED1352. Thus, up grading from SED1352 to 1353 is easy in terms of both hardware and software.

The following list main difference between SED1353 and SED1352. For detailed specifications, refer to respective technical manual.

● Functional Comparison

Specifications	SED1353	SED1352
Color display	• 4/16/256 colors	• Not available
Monochrome display	• black/white binary. • 4/16-level gray scale.	• Not available. • 4/16-level gray scale.
Display data format	• 4/8 bits single/dual monochrome. • 4/8/16 bits signal/dual color.	• 4/8 bits single/dual monochrome. • Not available.
Setup of vertical scan period done in horizontal direction	Programmable.	Not available.
Look-up Table	• 3 × 16, 4-bit width.	• 1 × 16, 4-bit width.

● Modifications or Additions done on the Internal Register

(See SED1353 technical manual for the detail)

AUX [01h]
- bit 2 LCD Data Width bit 0
- bit 3 Gray Shade/Color

AUX [03h]
- bit 1 Color Mode
- bit 2 BW/256 colors

AUX [0Ch]
- bit 0:7 Horizontal Non-Display Period

AUX [0Eh]
- bit 4 ID Bit/RGB Index Bit 0
- bit 5 ID Bit/RGB Index Bit 1
- bit 6 Green Bank Bit 0
- bit 7 Green Bank Bit 1

AUX [0Fh]
- bit 4 Blue Bank Bit 0
- bit 5 Blue Bank Bit 1
- bit 6 Red Bank Bit 0
- bit 7 Red Bank Bit 1

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