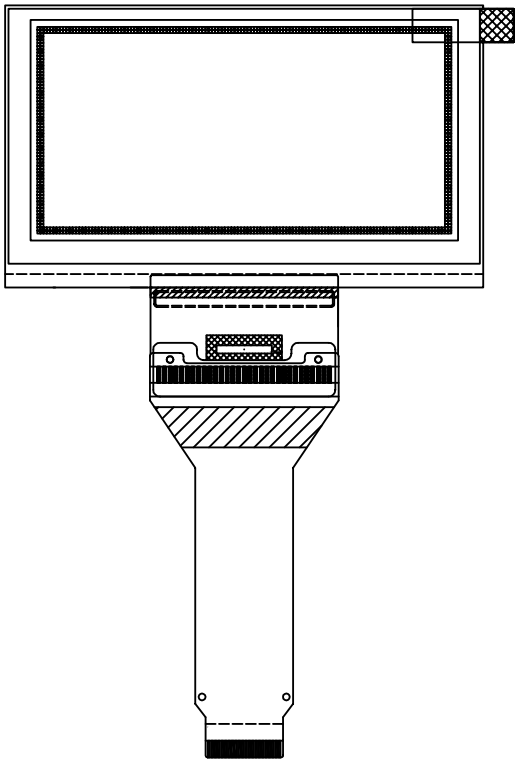
HANTRONIX

PRODUCT SPECIFICATION

HDR12864-L

128 x 64 MONOCHROME GRAPHICS OLED DISPLAY MODULE



HANTRONIX, INC. 10080 BUBB RD. CUPERTINO, CA 95014	Q.A.: ZW	REV.: 1.0	HDR12864-L	SHEET 1 OF 18 DATE: 8/24/09

FEATURES

- Small molecular organic light emitting diode.
- Color : Yellow
- Panel matrix : 128x64
- Driver IC : SSD1305
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 2.01mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface, I^2C interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 64 (H)	dot
2	Dot Size	0.45 (W) x 0.45 (H)	mm^2
3	Dot Pitch	0.48 (W) x 0.48 (H)	mm^2
4	Aperture Rate	88	%
5	Active Area	61.41 (W) x 30.69 (H)	mm^2
6	Panel Size	70.9 (W) x 41.86 (H)	mm^2
7	Panel Thickness	2.01	mm
8	Module Size	70.9 (W) x 111.61 (H) x 2.01 (T)	mm^3
9	Diagonal A/A size	2.7	inch
10	Module Weight	13 ± 10%	gram

MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	8	16	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	40,000	-	Hrs	120 cd/m², 50% checkerboard	Note (1)
Life Time	48,000	-	Hrs	100 cd/m², 50% checkerboard	Note (2)
Life Time	60,000	-	Hrs	80 cd/m², 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 15VDC, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m² :

- Contrast setting : 0xF0H
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 100 cd/m² :

- Contrast setting : 0xA7H
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 80 cd/m² :

- Contrast setting : 0x60H
- Frame rate : 105Hz
- Duty setting : 1/64

ELECTRICAL CHARACTERISTICS

D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)	-	14.5	15	15.5	V
V_{DD}	Digital power supply	-	2.4	2.7	3.5	V
V_{DDIO}	Logic Supply Voltage for MCU interface	-	1.6	-	V_{DD}	V
I_{DD}	Operating current for V_{DD} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA, No panel attached, All Display ON	Contrast=FFh	-	100	300	uA
I_{CC}, SLEEP I_{DD}, SLEEP I_{DDIO}, SLEEP	Sleep mode Current	V_{DD}= 2.4 V~3.5V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
I_{CC}	Operating current for V_{CC} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA, No panel attached, All Display ON	Contrast=FFh	-	550	1000	uA
V_{IH}	High logic input level	-	0.8* V_{DDIO}	-	-	V
V_{IL}	Low logic input level	-	0	-	0.2* V_{DDIO}	V
V_{OH}	High logic output level	I_{OUT} = 100uA, 3.3MHz	0.9* V_{DDIO}	-	-	V
V_{OL}	Low logic output level	I_{OUT} = 100uA, 3.3MHz	0	-	0.1* V_{DDIO}	V
I_{SEG}	Segment Output Current V_{DD}=2.7V, V_{CC}=12V, I_{REF}=10uA, Display on,	Contrast=FFh	294	320	346	uA
		Contrast=AFh	-	220	-	uA
		Contrast=7Fh	-	159	-	uA
		Contrast=3Fh	-	79	-	uA
		Contrast=0Fh	-	19	-	uA

ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		28	30	mA	All pixels on (1)
Standby mode current		3	5	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		420	450	mW	All pixels on (1)
Standby mode power consumption		45	75	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	80	100		cd/m^2	Display Average
Standby mode Luminance		60		cd/m^2	Display Average
CIEx (Yellow)	0.43	0.47	0.51		x, y (CIE 1931)
CIEy (Yellow)	0.45	0.49	0.53		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

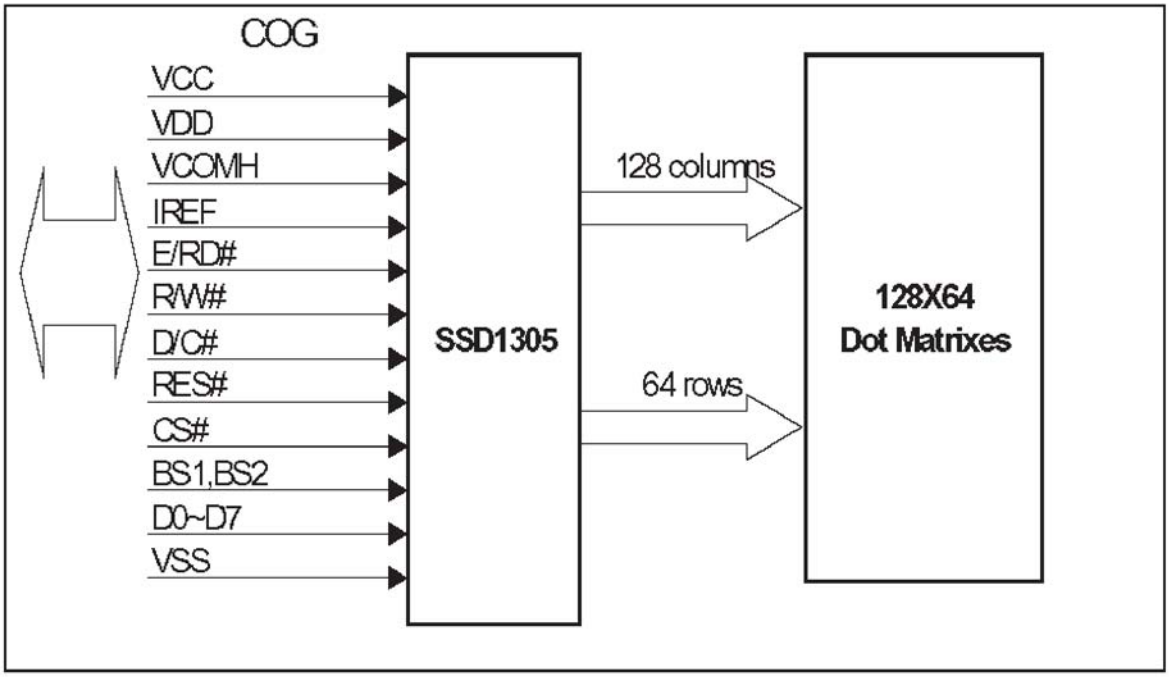
- Driving Voltage : 15VDC
- Contrast setting : 0xA7H
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

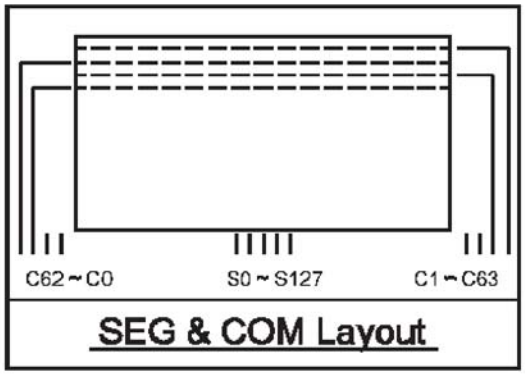
- Driving Voltage : 15VDC
- Contrast setting : 0x10H
- Frame rate : 105Hz
- Duty setting : 1/64

INTERFACE

FUNCTION BLOCK DIAGRAM



PANEL LAYOUT DIAGRAM



PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
VCC	1	Power supply for analog circuit.
VCOMH	2	Com Voltage Output. A capacitor should be connected between this pin and VSS.
IREF	3	Reference current input pin. A resistor should be connected between this pin and VSS.
D7	4	Data bus.
D6	5	Data bus.
D5	6	Data bus.
D4	7	Data bus.
D3	8	Data bus.
D2	9	Data bus.
D1	10	Data bus.
D0	11	Data bus.
E/RD#	12	Data read operation is initiated when it' s pull low.
R/W#	13	Data write operation is initiated when it' s pull low.
D/C#	14	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
RES#	15	Reset signal input. When it' s low, initialization of SSD1305 is executed.
CS#	16	Chip select input.
BS2	17	Interface select pin.
BS1	18	Interface select pin.
VDD	19	Power supply for logic circuit.
NC	20	No connection.
VSS	21	Ground.
VSS	22	Ground.

GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132x64= 8448bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

OUT	Row Address Direction='1'	Row Address Direction='0'			OUT	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG128	SEG129	SEG130	SEG131
					Column Address Remap='1'	0x83h	0x82h	0x81h	0x80h	0x7Fh	0x7Eh	0x7Dh	0x7Ch		0x03h	0x02h	0x01h	0x00h
					Column Address Remap='0'	0x00h	0x01h	0x02h	0x03h	0x04h	0x05h	0x06h	0x07h		0x80h	0x81h	0x82h	0x83h
COM0	0x3Fh	0x00h	PAGE 0		D0													
COM1	0x3Eh	0x01h			D1													
COM2	0x3Dh	0x02h			D2													
COM3	0x3Ch	0x03h			D3													
COM4	0x3Bh	0x04h			D4													
COM5	0x3Ah	0x05h			D5													
COM6	0x39h	0x06h			D6													
COM7	0x38h	0x07h			D7													
COM8	0x37h	0x08h	PAGE 1		D0			■	■	■	■							
COM9	0x36h	0x09h			D1		■					■						
COM10	0x35h	0x0Ah			D2		■					■						
COM11	0x34h	0x0Bh			D3		■					■						
COM12	0x33h	0x0Ch			D4		■					■						
COM13	0x32h	0x0Dh			D5		■					■						
COM14	0x31h	0x0Eh			D6		■					■						
COM15	0x30h	0x0Fh			D7			■	■	■	■							
COM16	0x2Fh	0x10h	PAGE 2		D0													
COM17	0x2Eh	0x11h			D1													
COM18	0x2Dh	0x12h			D2													
COM19	0x2Ch	0x13h			D3													
COM20	0x2Bh	0x14h			D4													
COM21	0x2Ah	0x15h			D5													
COM22	0x29h	0x16h			D6													
COM23	0x28h	0x17h			D7													
.																		
.																		
COM48	0x0Fh	0x30h	PAGE 6		D0													
COM49	0x0Eh	0x31h			D1													
COM50	0x0Dh	0x32h			D2													
COM51	0x0Ch	0x33h			D3													
COM52	0x0Bh	0x34h			D4													
COM53	0x0Ah	0x35h			D5													
COM54	0x09h	0x36h			D6													
COM55	0x08h	0x37h			D7													
COM56	0x07h	0x38h	PAGE 7		D0													
COM57	0x06h	0x39h			D1													
COM58	0x05h	0x3Ah			D2													
COM59	0x04h	0x3Bh			D3													
COM60	0x03h	0x3Ch			D4													
COM61	0x02h	0x3Dh			D5													
COM62	0x01h	0x3Eh			D6													
COM63	0x00h	0x3Fh			D7													

INTERFACE TIMING CHART

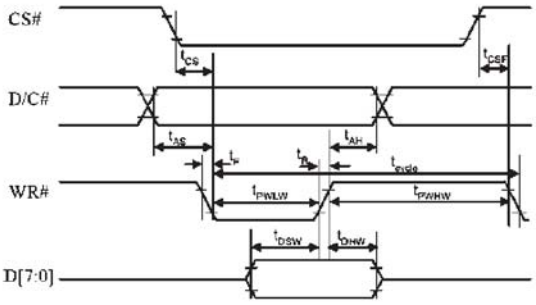
8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = V_{DD}, T_A = 25°C)

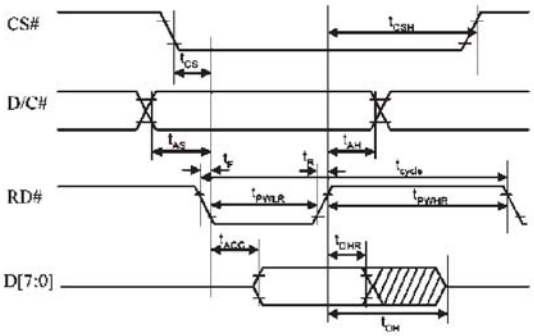
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)

Write cycle (Form 1)

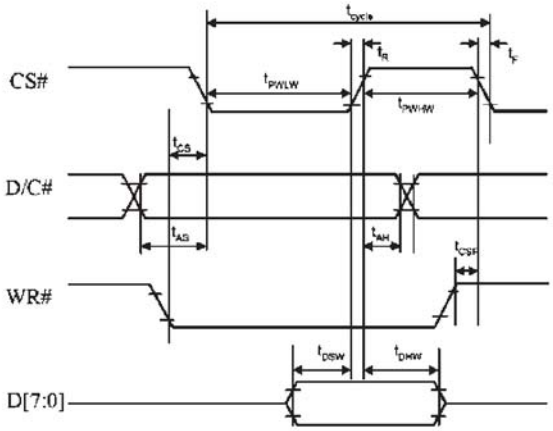


Read cycle (Form 1)

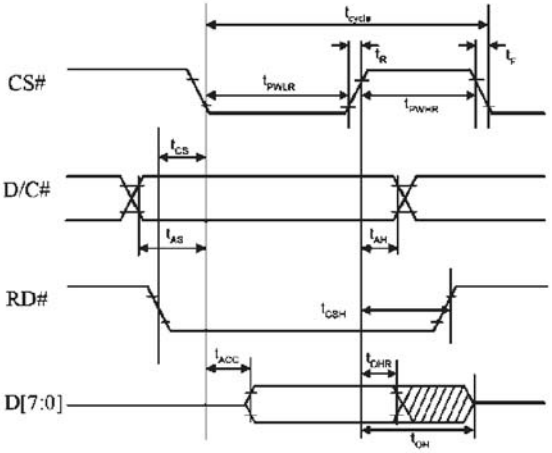


8080-series parallel interface characteristics (Form 2)

Write cycle (Form 2)



Read cycle (Form 2)

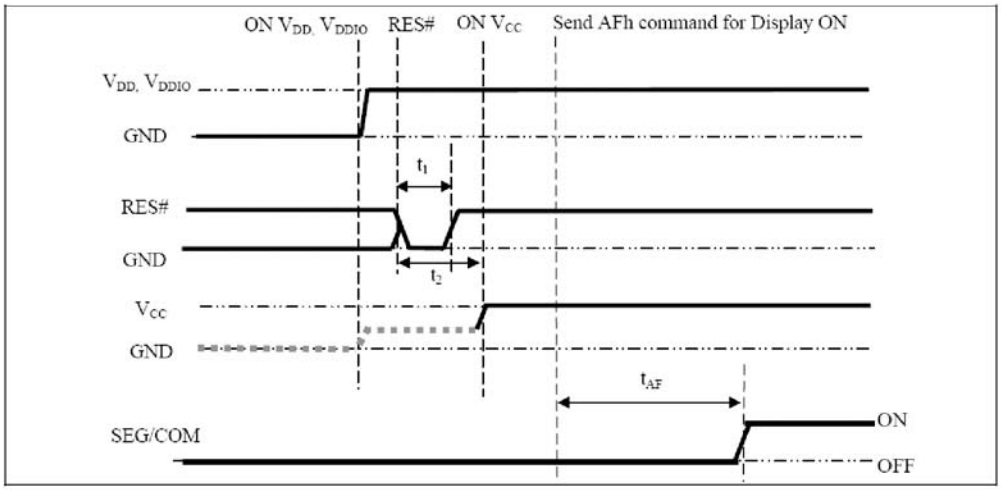


POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

POWER ON / OFF SEQUENCE

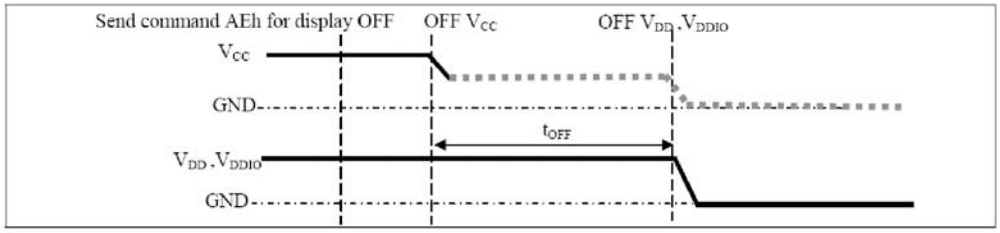
Power ON sequence:

1. Power ON V_{DD}, V_{DDIO}.
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

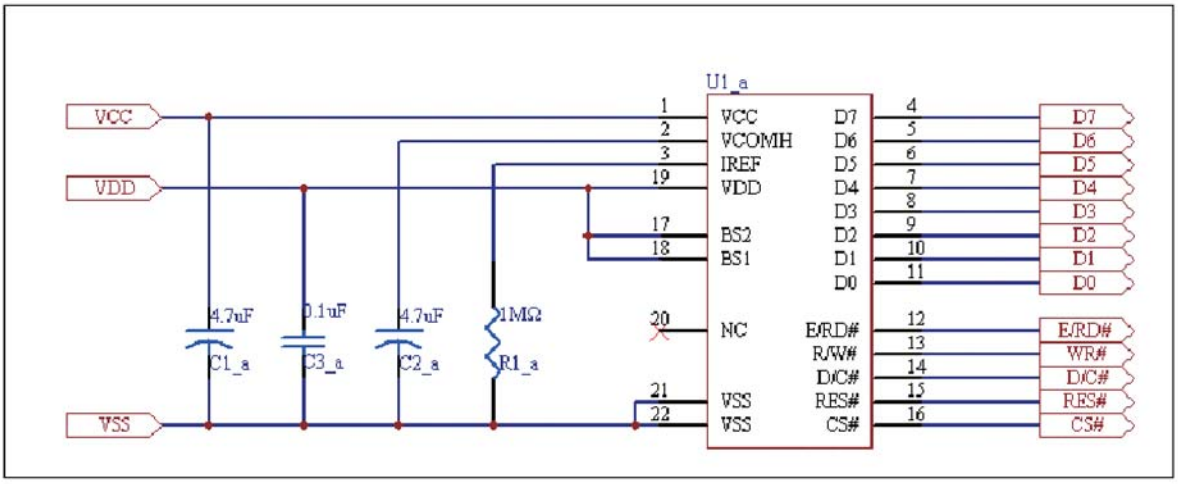


Note:

(1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

APPLICATION CIRCUIT



COMMAND TABLE

Refer to SSD1305 IC Spec.

RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

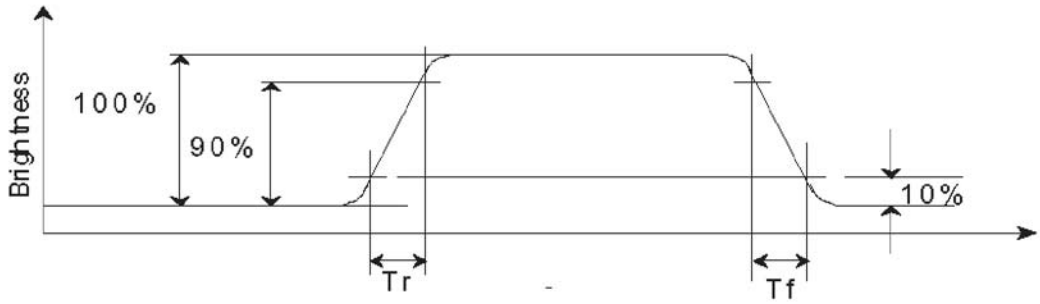


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

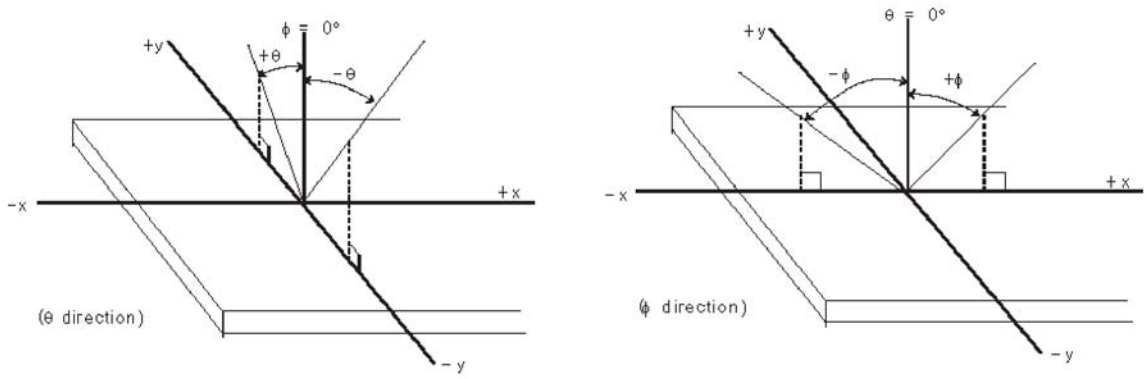
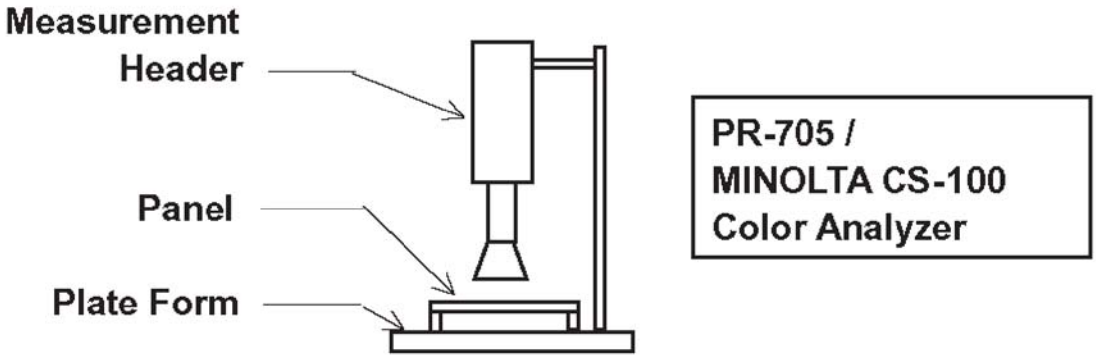


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

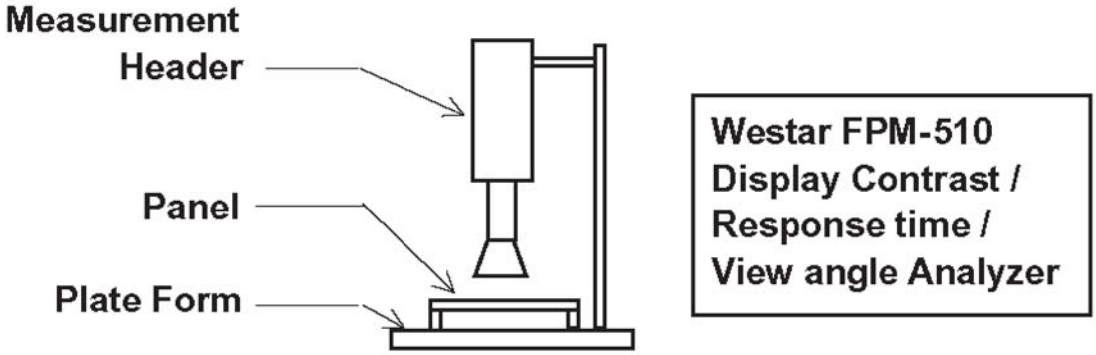
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

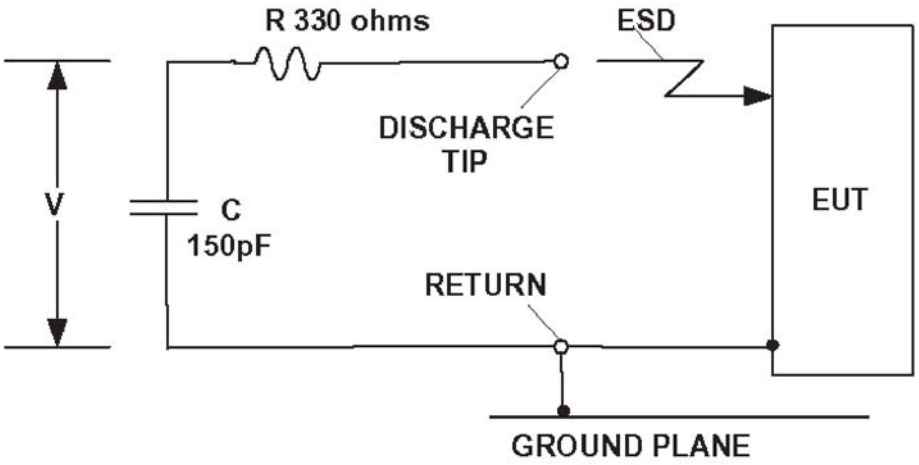


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



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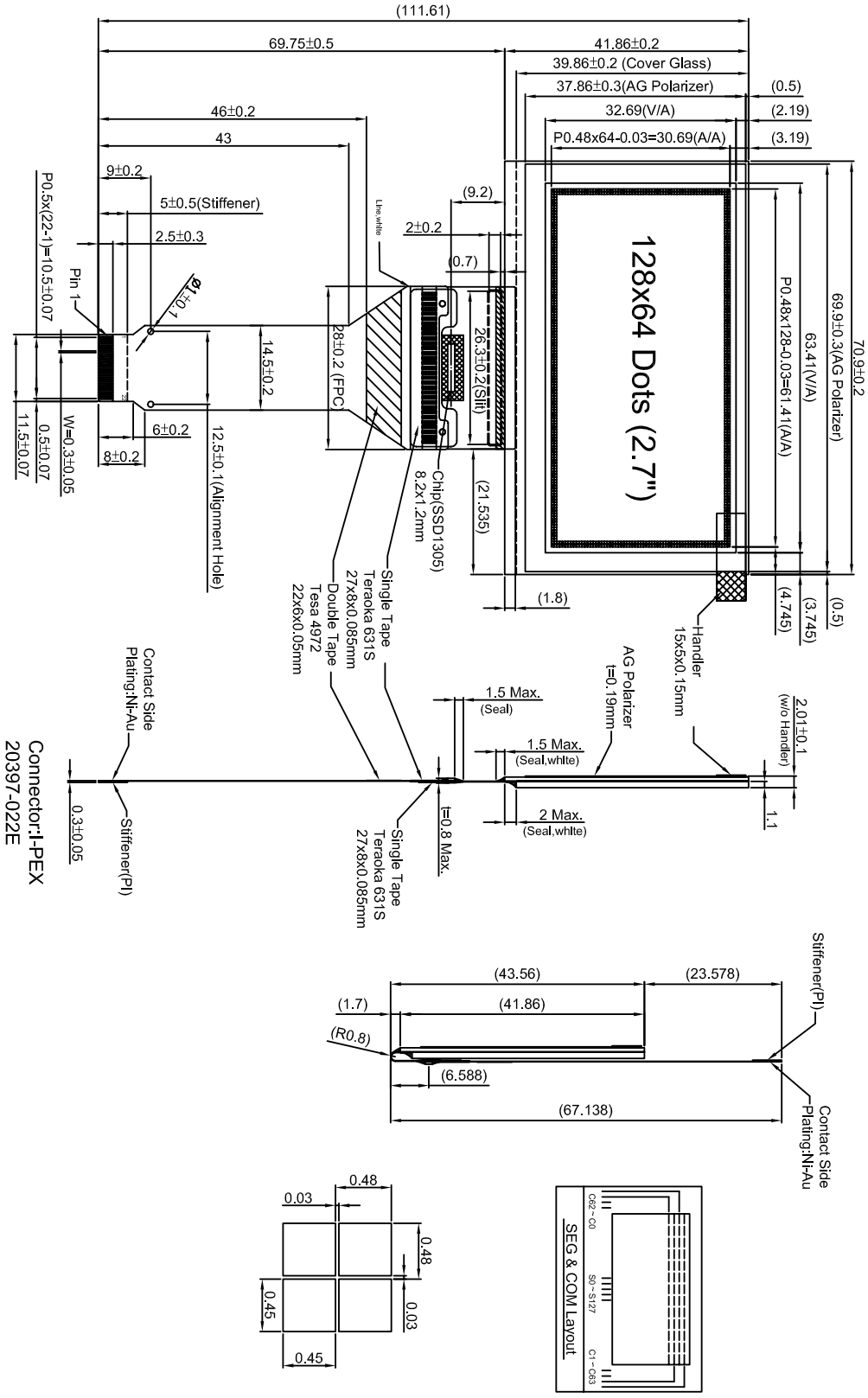

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