Interfacing a Hantronix 128x64 Graphic Module to an 8-bit Microcontroller

Introduction:
Due to its thin profile, light weight, low power consumption and easy handling, liquid crystal graphic display modules are used in a wide variety of applications. This note details a simple interface technique between a Hantronix HDM64GS12 and a micro-controller. The HDM64GS12 has a built-in Hitachi HD61202, or Samsung KS107, controller which performs all of the refreshing and data storage tasks of the LCD display. This note applies to any display using these controllers. The driving micro-controller is the popular 87C751.

The display is split logically in half. It contains two controllers with controller #1 (Chip select 1) controlling the left half of the display and controller #2 (Chip select 2) controlling the right half. Each controller must be addressed independently.

The page addresses, 0-7, specify one of the 8 horizontal pages which are 8 bits (1 byte) high. A drawing of the display and how it is mapped to the refresh memory is shown below.

The schematic on page two is a simple circuit to illustrate one possible interface scheme. This is the circuit that the code example will work with directly.
Schematic Diagram:

The following software is in 8051 assembly language and will run as-is on the hardware shown above. The busy status flag is not tested in this software. It is usually not necessary to do so when the display module is connected to the processor via I/O lines. When the module is connected to the processor’s data bus and mapped into it’s memory area the status should be tested to guarantee reliable service.

Displayed Pattern:
Software Flowchart:

Initialization Bytes:

**0c0h** Specifies the RAM line to be displayed at the top of the screen. Here it is line 0.

**040h** This is the column address. It specifies one of 64 possible columns. Here it is 0.

**0b8h** This is the page address. It specifies one of 8 possible pages. Here it is 0.

**03fh** Display on/off. 03fh turns it on and a 03eh turns it off.
The processor clock speed is 16MHz.
Cycle time is .750mS.
HD61202 demo software to display
the Hantronix logo on a 128 x 64 LCD.

; Initialize the 64gs12

Start:

; Display pattern

Loop1:

Loop2:

; SUBROUTINES

; Byte sends the byte pointed to by
; the DPTR to the graphics module
; as a series of data bytes.

Byte:

; WRITE sends the byte in R1 to the
display.

Write:

Write2:

Write1:

; end
;******************************************************************************
; TABLES AND DATA
;
; Initialization bytes

Msg1:
    db 0c0h,40h,0b8h,3fh,99h
; "Hantronix", left half

Msg1:
    db 0,0feh,10h,10h,10h,0feh,0 ;H
    db 0fch,12h,12h,12h,0fch,0 ;A
    db 0feh,08h,10h,0feh,0 ;N
    db 02h,02h,0feh,02h,02h,0 ;T
    db 0feh,12h,32h,52h,8ch,0 ;R
    db 7ch,82h,82h,82h,7ch,0 ;O
    db 0feh,08h,10h,20h,0feh,0 ;N
    db 0,0,82h,0feh,82h,0 ;I
    db 0,0c6h,28h,10h,28h,0c6h,0 ;X
    db 0,38h,7ch,0f8h,7ch,38h,0 ;heart
    db 0,99h
; "Hantronix", right half (reverse video)

Msg1r:
    db 0ffh,0c7h,83h,07h,83h,0c7h,0ffh ;heart
    db 0ffh,39h,0d7h,0efh,0d7h,39h,0ffh ;X
    db 0ffh,0ffh,7dh,01h,7dh,0ffh ;I
    db 01h,0dfh,0efh,0ffh,01h,0ffh ;N
    db 83h,7dh,7dh,83h,0ffh ;O
    db 073h,0adh,0cdh,0edh,01h,0ffh ;R
    db 0ffh,0f9h,0f9h,0f9h,0f9h,0f9h ;T
    db 01h,0dfh,0efh,0ffh,01h,0ffh ;N
    db 03h,0edh,0edh,0edh,03h,0ffh ;A
    db 0ffh,01h,0efh,0efh,0efh,01h,0ffh ;H
    db 0ffh,99h

end