HANTRONIX

PRODUCT SPECIFICATION

HDA700L-2SHL

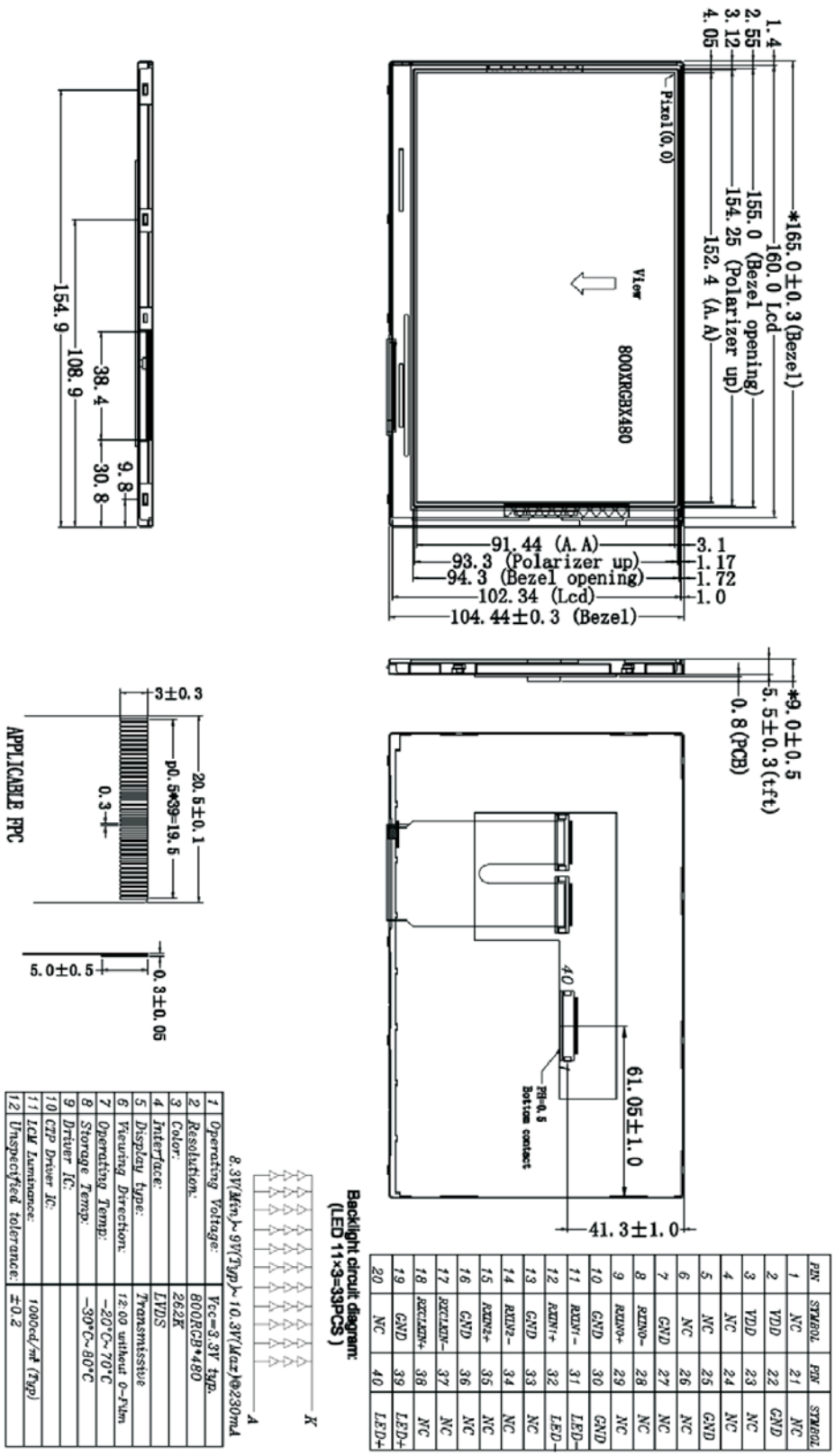
7”, TFT WVGA (800X480) COLOR LCD DISPLAY MODULE

HANTRONIX, INC. 10080 BUBB RD. CUPERTINO, CA 95014	Q.A.: Z.W.	REV.: 1.0	HDA700L-2SHL	SHEET 1 OF 18 DATE: 7/7/16

1. General Specifications

No	Item	Contents	Unit
1	Size	7.0	inch
2	Resolution	800RGB*480	
3	Interface	LVDS	
4	Color Depth	262K	
5	Technology Type	a-Si TFT	
6	Pixel size	0.1905*0.1905	mm
7	Pixel Arrangement	RGB Vertical Stripe	
8	Display Mode	Transmissive	
9	Surface Treatment	Anti-glare	
10	Viewing Direction	12:00	o'clock
11	LCM (W x H x D)	165*104.44*5.5	mm
12	Active Area (W x H)	152.4*91.44	mm
13	With/Without CTP	Without CTP	
14	LED Numbers	33	

2. Mechanical Drawing



PIN	SYMBOL	PIN	SYMBOL
1	NC	21	NC
2	VDD	22	GND
3	VDD	23	NC
4	NC	24	NC
5	NC	25	GND
6	NC	26	NC
7	GND	27	NC
8	RIN0-	28	NC
9	RIN0+	29	NC
10	GND	30	GND
11	RIN1-	31	LED-
12	RIN1+	32	LED-
13	GND	33	NC
14	RIN2-	34	NC
15	RIN2+	35	NC
16	GND	36	NC
17	RXCLKIN-	37	NC
18	RXCLKIN+	38	NC
19	GND	39	LED+
20	NC	40	LED+

1	Operating Voltage:	Vcc=3.3V typ.
2	Resolution:	800RGBW480
3	Color:	262K
4	Interface:	LVDS
5	Display type:	Transmissive
6	Viewing Direction:	12:00 without 0-Film
7	Operating Temp:	-20°C~70°C
8	Storage Temp:	-30°C~80°C
9	Driver IC:	
10	CTP Driver IC:	
11	LCM Luminance:	1000cd/m² (Typ)
12	Unspecified tolerance:	±0.2

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3. PIN Assignment

Pin No	Symbol	Function	Remark
1	NC	No connection	
2	VDD	Power Voltage for digital circuit	
3	VDD	Power Voltage for digital circuit	
4-6	NC	No connection	
7	GND	Ground	
8	RXIN0-	-LVDS differential data input	
9	RXIN0+	+LVDS differential data input	
10	GND	Ground	
11	RXIN1-	-LVDS differential data input	
12	RXIN1+	+LVDS differential data input	
13	GND	Ground	
14	RXIN2-	-LVDS differential data input	
15	RXIN2+	+LVDS differential data input	
16	GND	Ground	
17	RXCLKIN-	-LVDS differential clock input	
18	RXCLKIN+	+LVDS differential clock input	
19	GND	Ground	
20	NC	No connection	
21	NC	No connection	
22	GND	Ground	
23	NC	No connection	
24	NC	No connection	
25	GND	Ground	
26-29	NC	No connection	
30	GND	Ground	
31	LED-	LED Cathode	
32	LED-	LED Cathode	
33-38	NC	No connection	
39	LED+	LED Anode	
40	LED+	LED Anode	

4. Absolute Maximum Rating

AGND = GND = 0V , Ta = 25° C

Item	Symbol	Min	Max	Unit	Remark
Power Voltage	VCC	-0.3	4	V	
Backlight Forward Current	I_{LED}		25	mA	For each LED
Operating Temperature	T_{OPR}	-20	70	° C	
Storage Temperature	T_{STG}	-30	80	° C	

The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

5. Electrical Characteristics

5.1. Recommended Operating Condition

AGND = GND = 0V , Ta = 25° C

Item	Symbol	Min	Typ.	Max	Unit	Remark
Power Voltage	VCC	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	-	VCC	V	
Input logic low voltage	V_{IL}	GND	-	0.8	V	

5. 2.Rcommended Driving Condition for Backlight

Ta = 25° C

Item	Symbol	Min	Typ.	Max	Unit	Remark
Forward Voltage	Vf	8.3	9.0	10.3	V	
Forward Current	If		230		mA	
Operating Life Time	-	20000			Hours	

Note 1:The LED supply voltage is defined by the number of LED at Ta=25℃ and If=**230**mA.

Note 2:The "Operating Life Time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and If=**230**mA. The LED lifetime could be decreased if operating If is larger than **230** mA.

6. 2. Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			2.0	3.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			1.8	3.5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 *(Figure 11, Figure 12)*	f = 85 MHz	0.49	0.84	1.19	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.17	2.52	2.87	ns
RSPos2	Receiver Input Strobe Position for Bit 2		3.85	4.20	4.55	ns
RSPos3	Receiver Input Strobe Position for Bit 3		5.53	5.88	6.23	ns
RSPos4	Receiver Input Strobe Position for Bit 4		7.21	7.56	7.91	ns
RSPos5	Receiver Input Strobe Position for Bit 5		8.89	9.24	9.59	ns
RSPos6	Receiver Input Strobe Position for Bit 6		10.57	10.92	11.27	ns
RSKM	RxIN Skew Margin (Note 4) *(Figure 13)*	f = 85 MHz	290			ps
RCOP	RxCLK OUT Period *(Figure 5)*		11.76	T	50	ns
RCOH	RxCLK OUT High Time *(Figure 5)*	f = 85 MHz	4.5	5	7	ns
RCOL	RxCLK OUT Low Time *(Figure 5)*		4.0	5	6.5	ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 5)*		2.0			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 5)*		3.5			ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 3.3V *(Figure 6)*		5.5	7.0	9.5	ns
RPLLS	Receiver Phase Lock Loop Set *(Figure 7)*				10	ms
RPDD	Receiver Power Down Delay *(Figure 10)*				1	µs

Note 4: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 150 ps).

6. 3. AC Timing Diagrams

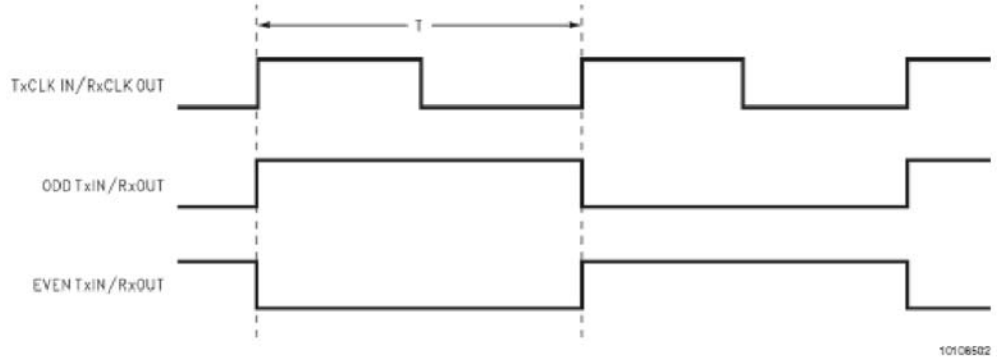


FIGURE 1. "Worst Case" Test Pattern

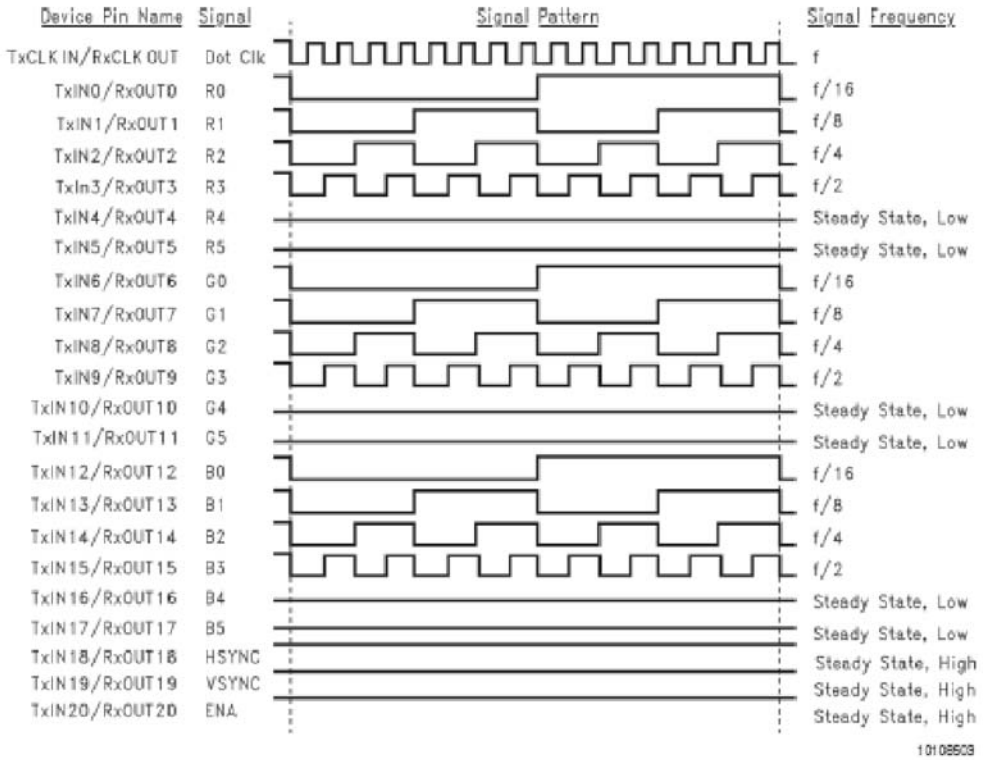


FIGURE 3. "16 Grayscale" Test Pattern (DS90CF366)(Notes 5, 6, 7, 8)

Note 5: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 6: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 7: *Figures 1, 3* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 8: Recommended pin to signal mapping. Customer may choose to define differently.

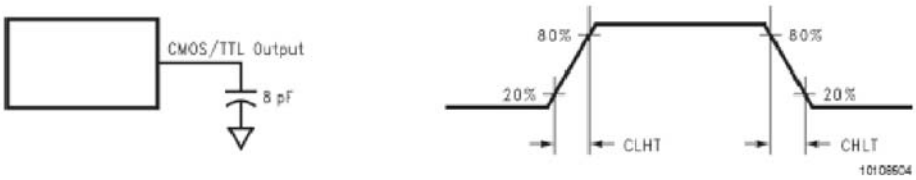


FIGURE 4. DS90CF386/DS90CF366 (Receiver) CMOS/TTL Output Load and Transition Times

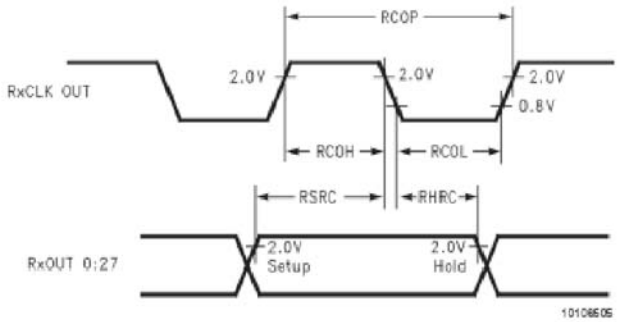


FIGURE 5. DS90CF386/DS90CF366 (Receiver) Setup/Hold and High/Low Times

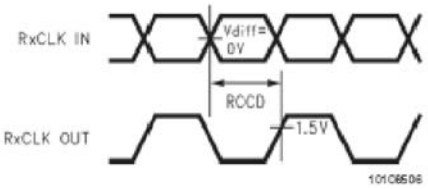


FIGURE 6. DS90CF386/DS90CF366 (Receiver) Clock In to Clock Out Delay

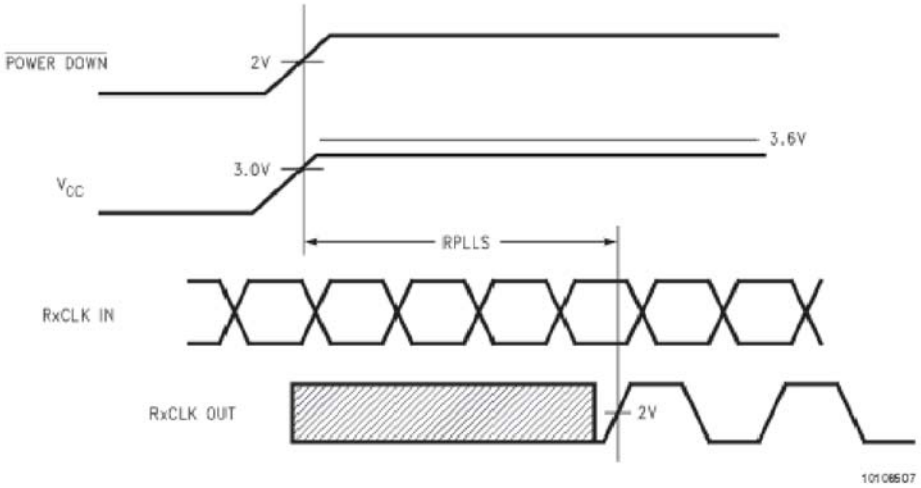


FIGURE 7. DS90CF386/DS90CF366 (Receiver) Phase Lock Loop Set Time

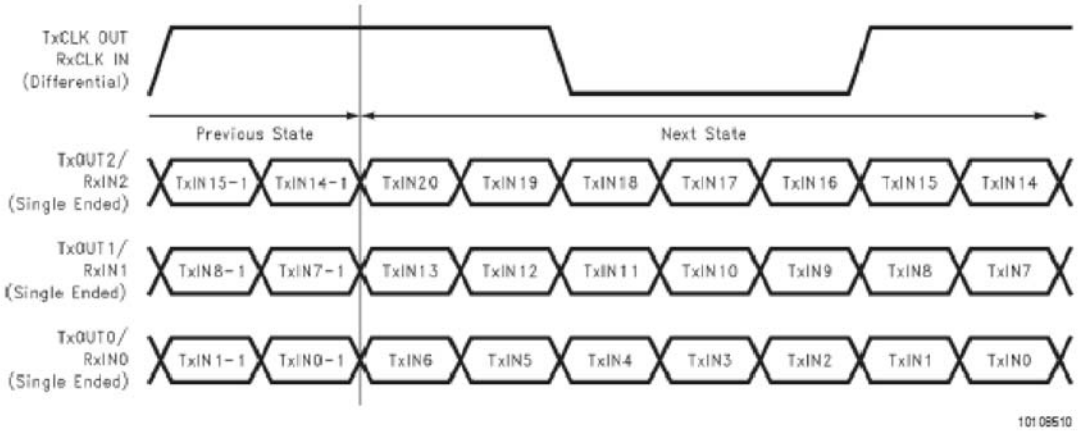


FIGURE 9. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CF366

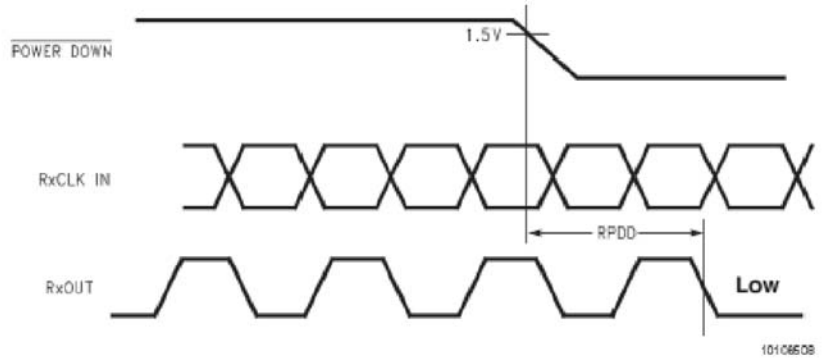


FIGURE 10. DS90CF386/DS90CF366 (Receiver) Power Down Delay

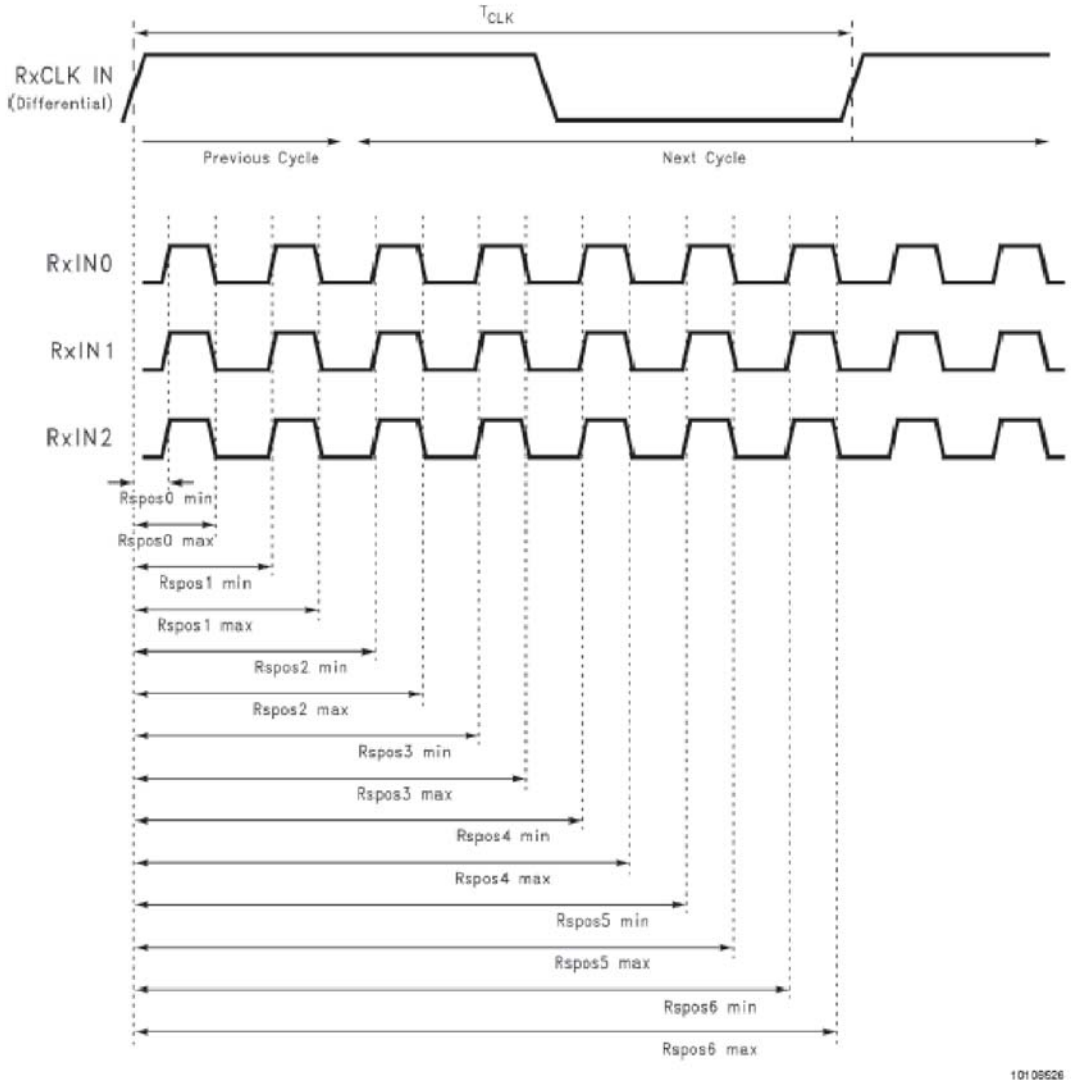
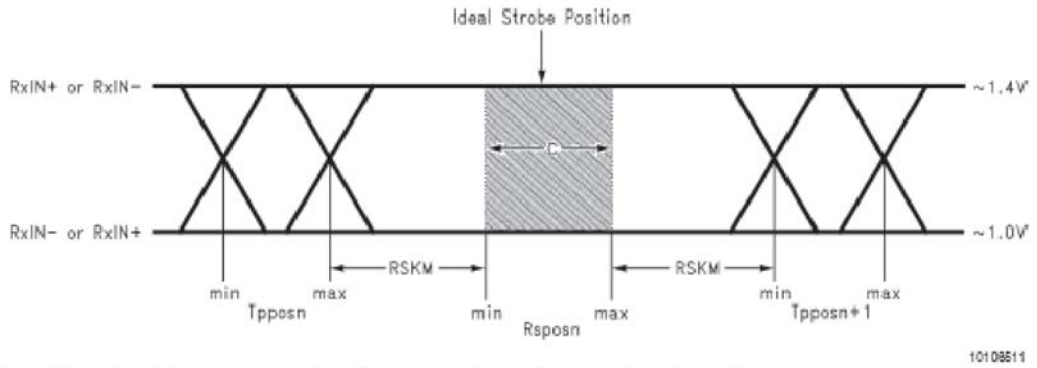


FIGURE 12. DS90CF366 (Receiver) LVDS Input Strobe Position



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

Tppos — Transmitter output pulse position (min and max)

RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) (Note 9) + ISI (Inter-symbol interference) (Note 10)

Cable Skew — typically 10 ps–40 ps per foot, media dependent

Note 9: Cycle-to-cycle jitter is less than 250 ps at 85 MHz.

Note 10: ISI is dependent on interconnect length; may be zero.

FIGURE 13. Receiver LVDS Input Skew Margin

7. Optical Characteristics

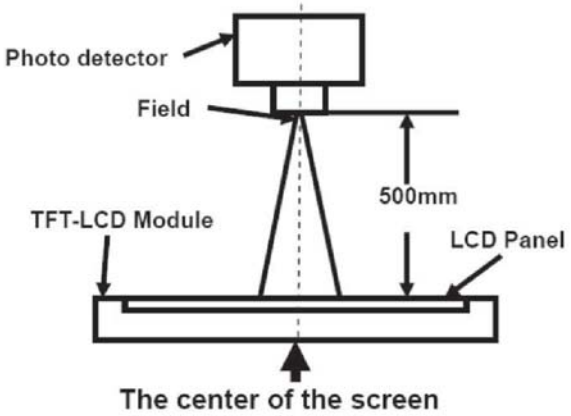
Item		Symbol	Condition	Min	Typ.	Max	Unit	Remark
View Angles		θ L	CR≥10	65	70	-	Degree	Note 2
		θ R		65	70	-		
		θ T		55	60	-		
		θ B		55	60	-		
Contrast Ratio		CR	θ = 0°	250	400	-	-	Note 1 Note 3
Response Time		T_{ON}	25° C	-	5	10	ms	Note 1 Note 4
		T_{OFF}		-	11	16		
Chromaticity	W_x	x			0.31			Note 1 Note 5
	W_y	y			0.33			
Uniformity		U		70	75		%	Note 5
Luminance		L		-	1000	-	cd/m^2	Note 1 Note 5

Test Conditions:

1. If=230 mA(Backlight current), VCC =3.3 V, the ambient temperature is 25° C.
2. The test systems refer to Note 2.

Note 1: Definition of optical measurement system.

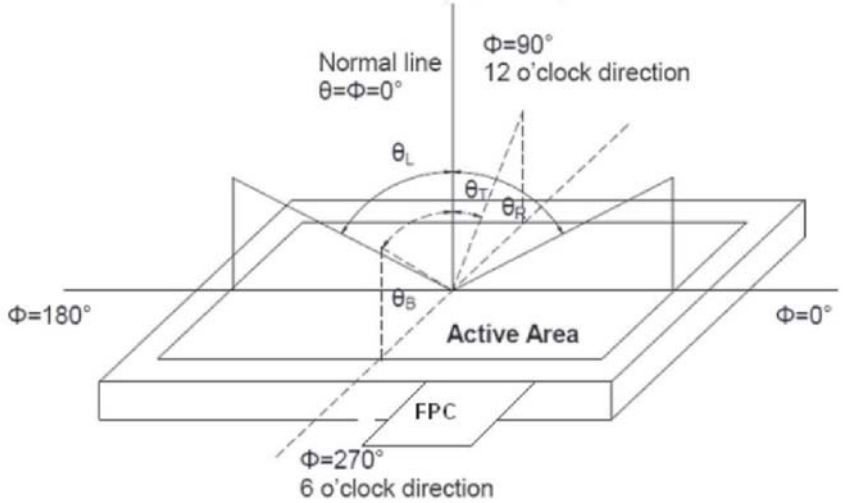
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	BM-5A	1°
Luminance		
Lum Uniformity		
Chromaticity	SR-3A	
Response Time	TRD100	-

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

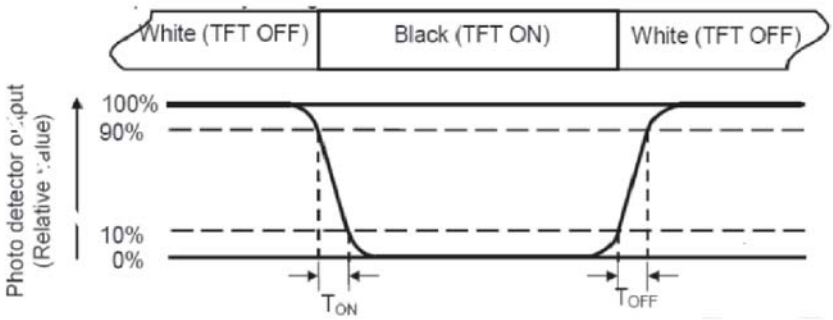
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

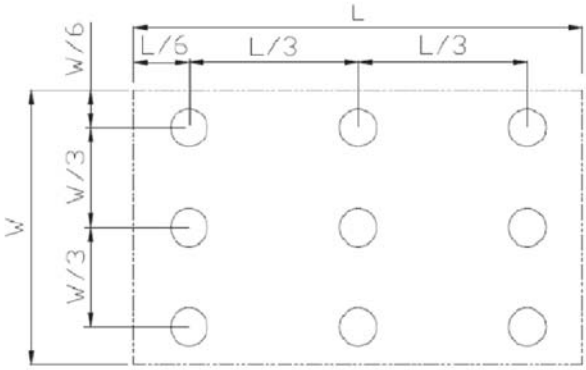
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

8. Environmental/Reliability Test

No.	Test Item	Test Condition	Inspection after test
1	High Temperature Storage	80±2℃/240 hours	Inspection after 2~4hours storage at room temperature,the sample shall be free from defects: 1.Air bubble in the LCD; 2.Sealleak; 3.Non-display; 4.missing segments; 5.Glass crack; 6.Current Idd is twice higher than initial value.
2	Low Temperature Storage	-30±2℃/240 hours	
3	High Temperature Operating	70±2℃/240 hours	
4	Low Temperature Operating	-20±2℃/240 hours	
5	Temperature Cycle	-20℃~ 25℃~ 70℃ × 10cycles (30min.) (5min.) (30min.)	
6	Damp Proof Test	60℃±5℃×90%RH/240 hours	
7	Vibration Test	Frequency：10Hz~55Hz~10Hz Amplitude：1.5mm, X，Y，Z direction for total	
8	Dropping test	Drop to the ground from 1m height, one time, every side of carton. (Packing condition)	
9	ESD test	Voltage:±8KV R: 330Ω C: 150pF Air discharge, 10time	

Remark:
1.The test samples should be applied to only one test item.
2.Sample size for each test item is 5~10pcs.
3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5.EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
7.Please use automatic switch menu(or roll menu) testing mode when test operating mode.

10. Standard Specifications For Product Quality

10.1. Manner of test:

10.1.1 The test must be under 40W fluorescent light, and the distance of view must be at 30±10cm.

10.1.2 Room temperature 25±5℃ Humidity: (60±10)%RH.

10.2. Quality specification

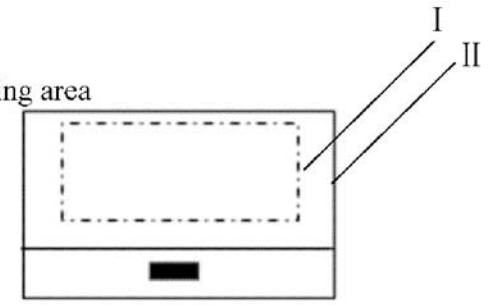
It shall be based on GB2828-87, inspection level II .

	IETM	CHECK LEVEL	AQL
MAJOR (MA)	1.Liquid crystal leakage 2.Wrong polarizer 3.Outside dimension 4. Bright dot、Dark dot 5. Display abnormal 6. Class crack	II	0.25
MINOR (MI)	1. Spot Defect (Including black spot、white spot、pinhole、foreign particle、bubbles、hurt） 2. fragment 3. Line Defect (Including black line、white line、cratch) 4. Incision defect 5. Newton's ring 6. Other visual defects	II	1.0

10.3. Definition of area:

10.3.1 Ⅰ area: viewing area

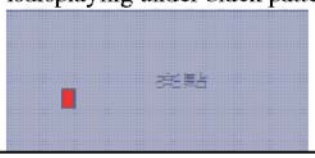
Ⅱ area: outside viewing area

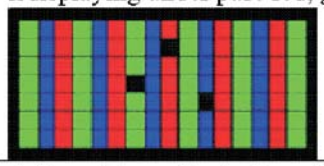


10.4. Standard of appearance test for Ⅰ area: (unit: mm)

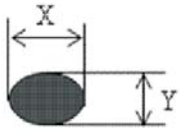
NOTE: Defect ignore for Ⅱ area .

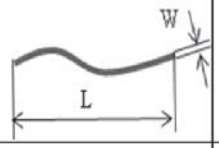
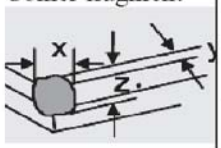
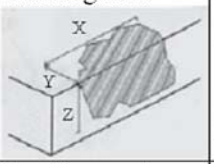
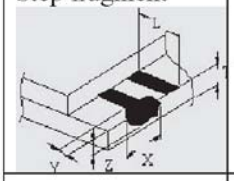
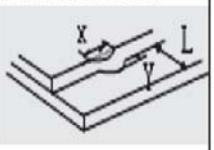
10.4.1 Bright/Dark Dots explain

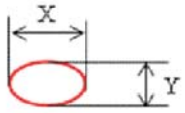
Name	Explain	Definition
Bright dot	Dots appear bright and unchanged in size in which LCD panel isdisplaying under black pattern 	The definition of dot: The size of a defective dot over 1/2 of single pixel dot is regarded as one defective dot . NOTE: One pixel

Dark dot	Dots appear dark and unchanged in size in which LCD panel isdisplaying under pure red, green, blue pattern. 	consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)
ADJACENT DOT	Adjacent two sub-pixel are defect（define two dot defect）	

10.4.2 Inspection standard

№	Items	Criterion		Checking Manner	Defect Classes
1	Bright/dark dot	Under 6” (contain 6”)	Bright dot：2 Dark dot：N≤4 **Note:** be more than 5mm apart	Checking with eyes	MAJ
		6”-12”	Bright dot：N≤4 Dark dot：N≤5 Total Bright and Dark Dots：N≤8 **Note ：** 1.Two bright dot defects (red, green, blue, and white) should be larger than 15mm; 2.The distance between black dot defects or black and bright dot defects should be more than 5mm apart.		
2	Spot Defect (Including black spot.white spot. Pinhole.foreign particle.bubbles.hurt）  D=(X+Y)/2	Under 6” （contain 6”）	D≤0.1 Ignore 0.1＜D≤0.35 N≤3 0.35＜D N=0	Checking with eyes	MIN
		6”-12”	D≤0.3 Ignore 0.3＜D≤0.6 N≤4 0.6＜D N=0		

№	Items	Criterion		Checking manner	Defect classes
3	Line Defect (Including black Line.white line. scratch) 	Under 6" (contain 6")	W≤0.02 Ignore 0.02＜W≤0.04 L≤5 N≤2 0.04＜W≤0.06 L≤5 N≤1 W＞0.06 N=0	Checking with eyes	MIN
		6"-12"	W≤0.07 Ignore 0.07＜W≤0.1 L≤10 N≤4 W＞0.1 N=0		
4	Display abnormal	Not allowed		Checking with eyes	MAJ
5	Outside dimension	Accord with drawing		Callipers	MAJ
6	Class crack	Not allowed		Checking with eyes	MAJ
7	Leak	Not allowed		Checking with eyes	MAJ
8	Comer fragment 	X≤3 Y≤3 Z≤T Ignore Note ： 1.No hurt identifying .wire.seal 2.T：Glass thickness X: Length Y: Width Z: thickness		Checking with eyes	MIN
9	Side fragment 	Y≤1 Z≤T Ignore Note ： 1.No hurt identifying .wire.seal 2.T：Glass thickness X: Length Y: Width Z: thickness		Checking with eyes	MIN
	Step fragment 	Y≤1 and Y≤1/4 L		Checking with eyes	MIN
	Incision defect 	Y≤1 and accord with outside dimension		Checking with eyes	MIN

№	Items	Criterion		Checking manner	Defect classes
10	Newton's ring (CTP or Cover board)  D=(X+Y)/2	Under 6" (contain 6")	D≤25 N≤3 D＞25 N=0	Checking with eyes	MIN
		6"-12"	D≤70 N≤5 D＞70 N=0		