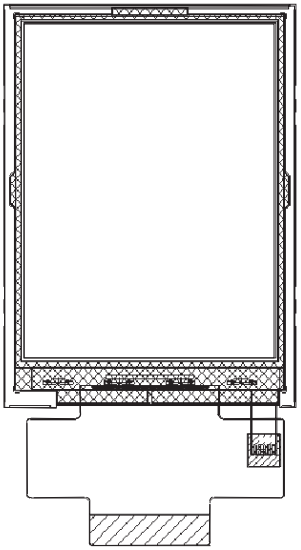
HANTRONIX

PRODUCT SPECIFICATION

HDA280-6S1

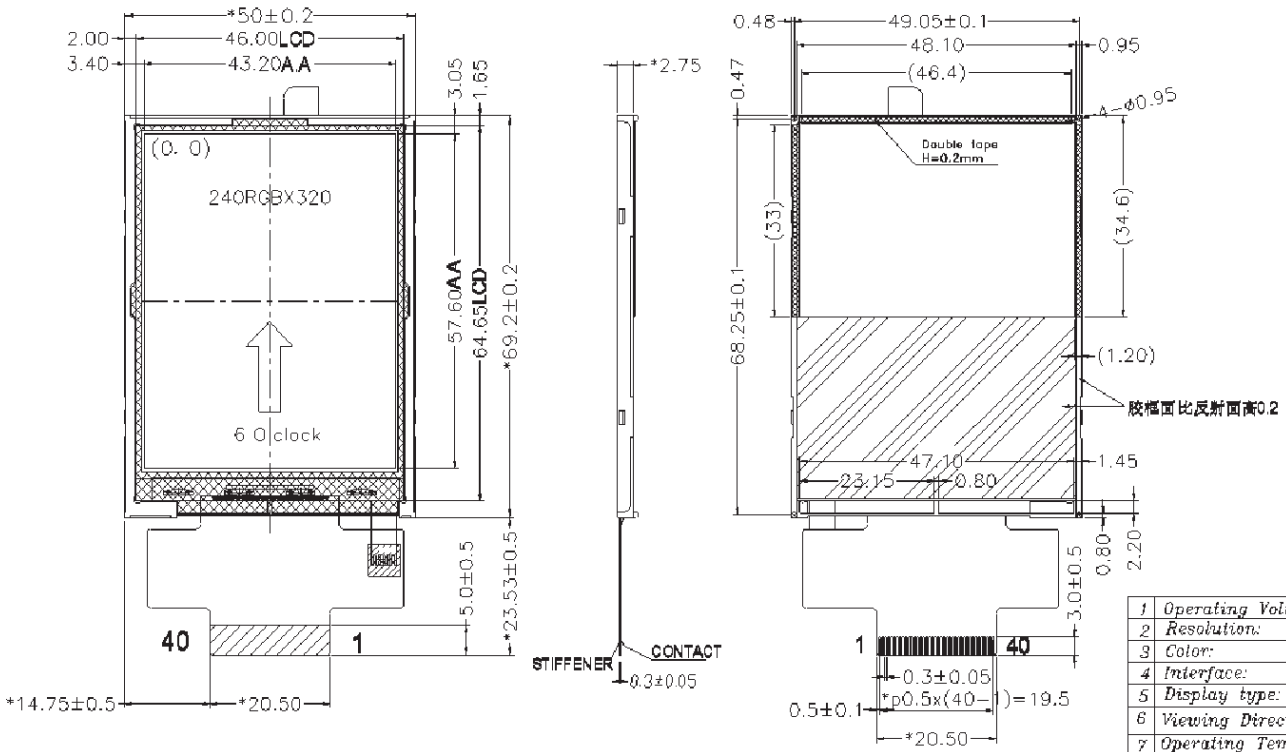
2.8”, 240x320 TFT COLOR GRAPHICS LCD DISPLAY MODULE



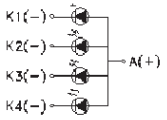
HANTRONIX, INC. 10080 BUBB RD. CUPERTINO, CA 95014	Q.A.: Z.W.	HDA280-6S1	SHEET 1 OF 21 DATE: 3/8/18

1. General Specifications

No	Item	Contents	Unit
1	Size	2.8	inch
2	Resolution	240RGB*320	
3	Interface	Serial,Parallel	
4	Color Depth	262k	
5	Technology Type	a-Si TFT	
6	Pixel Pitch	0.18X0.18	mm
7	Pixel Arrangement	RGB Vertical Stripe	
9	Display Mode	Transmissive	
10	Viewing Direction	6:00	o'clock
11	LCM (W x H x D)	50*69.2*2.75	mm
12	Active Area (W x H)	43.20*57.60	mm
13	With/Without TSP	Without TSP	
14	LED Numbers	4	



1	LEDK2	21	DB9
2	LEDK1	22	DB10
3	LEDA	23	DB11
4	VDDI	24	DB12
5	VDD	25	DB13
6	GND	26	DB14
7	CSX	27	DB15
8	DCX	28	DB16
9	WRX	29	DB17
10	RDX	30	SDO
11	RESX	31	SDA
12	DB0	32	NC
13	DB1	33	NC
14	DB2	34	IM0
15	DB3	35	IM1
16	DB4	36	IM2
17	DB5	37	NC
18	DB6	38	NC
19	DB7	39	NC
20	DB8	40	NC



BACK LIGHT CIRCUIT

1	Operating Voltage:	VDD=2.8V(typ.),VDDI=1.8V(typ.)
2	Resolution:	240RGB*320
3	Color:	262k
4	Interface:	Serial,Parallel
5	Display type:	Transmissive
6	Viewing Direction:	6:00
7	Operating Temp:	-30°C~70°C
8	Storage Temp:	-30°C~80°C
9	Backlight:	3.3V(typ.),80mA
10	Surface Luminance:	300cd/m2(typ.)
11	Driver IC:	ST7789V
12	Unspecified tolerance:	±0.2

SHEET 3 OF 21

DATE: 3/8/18

HDA280-6S1

Q.A.: Z.W.

HANTRONIX, INC.
10080 BUBB RD.
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3. PIN Assignment

Pin No	Symbol	I/O	Function	Remark
1	LEDK2	P	LED backlight cathode	
2	LEDK1	P	LED backlight cathode	
3	LEDA	P	LED backlight anode	
4	VDDI	I	Power Supply for I/O System.	
5	VDD	I	Power Supply for Analog, Digital System and Booster Circuit.	
6	GND	P	Ground	
7	CSX	I	-Chip selection pin Low enable. High disable.	
8	DCX	I	-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock. DCX='1': display data or parameter. DCX='0': command data.	
9	WRX	I	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND	
10	RDX	I	-Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND.	
11	RESX	I	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.	
12-29	DB0-DB17	I/O	-DB[17:0] are used as MCU parallel interface data bus. 8-bit I/F: when IM3:0, DB[7:0] are used; when IM3:1, DB[17:10] are used. 9-bit I/F: when IM3:0, DB[8:0] are used; when IM3:1, DB[17:9] are used. 16-bit I/F: when IM3:0, DB[15:0] are used; when IM3:1, DB[17:10] and DB[8:1] are used. 18-bit I/F: DB[17:0] are used. -DB[17:0] are used as RGB interface data bus. 6-bit RGB I/F: DB[5:0] are used. 16-bit RGB I/F: DB[17:13], DB[11:1] are used.	

Pin No	Symbol	I/O	Function	Remark
30	SDO	O	-SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	
31	SDA	I/O	-When IM3: Low, SPI interface input/output pin. -When IM3: High, SPI interface input pin. -The data is latched on the rising edge of the SCL signal. -If not used, please fix this pin at VDDI or DGND level.	
32	NC	-	No connection	
33	NC	-	No connection	
34-36	IM0,IM1,IM2	I		
37	NC	-	No connection	
38	NC	-	No connection	
39	NC	-	No connection	
40	NC	-	No connection	

IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin
1	0	0	0	80-16bit parallel I/F II	DB[17:10], DB[8:1]
1	0	0	1	80-8bit parallel I/F II	DB[17:10]
1	0	1	0	80-18bit parallel I/F II	DB[17:0].
1	0	1	1	80-9bit parallel I/F II	DB[17:9]
1	1	0	1	3-line 9bit serial I/F II	SDA: in/ SDO: out
1	1	1	0	4-line 8bit serial I/F II	SDA:in/ SDO: out

4. Absolute Maximum Rating

AGND = GND = 0V , Ta = 25° C

Item	Symbol	Min	Max	Unit	Remark
Power Voltage	VDD	-0.3	4.6	V	
	VDDI	-0.3	4.6		
Backlight Forward Current	I_{LED}		25	mA	For each LED
Operating Temperature	T_{OPR}	-30	70	° C	
Storage Temperature	T_{STG}	-30	80	° C	

The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

5. Electrical Characteristics

5.1. Recommended Operating Condition

AGND = GND = 0V , Ta = 25° C

Item	Symbol	Min	Typ.	Max	Unit	Remark
Power Voltage	VDD	2.4	2.8	3.3	V	
	VDDI	1.65	1.8	3.3		
Input logic high voltage	V_{IH}	0.7VDDI	-	VDDI	V	
Input logic low voltage	V_{IL}	VSS	-	0.3VDDI	V	

5. 2.Rcommended Driving Condition for Backlight

Ta = 25° C

Item	Symbol	Min	Typ.	Max	Unit	Remark
Forward Voltage	Vf	3.0	3.3	3.6	V	
Forward Current	If		80		mA	
Operating Life Time	-	50000			Hours	

Note 1:The LED supply voltage is defined by the number of LED at Ta=25℃ and If = 80 mA.

Note 2:The "Operating Life Time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and If = 80 mA. The LED lifetime could be decreased if operating If is larger than80 mA.

6. Timing Characteristics

6.1. AC Electrical Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

8080 Parallel Interface Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

18/16 Bits RGB Interface Timing Characteristics

6. 2. DC Electrical Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.4	2.8	3.3	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		12.2		14.97	V	Note 4
Gate Driver Low Voltage	VGL		-12.5		-7.16	V	
Gate Driver Supply Voltage		| VGH-VGL |	19.36		27.47	V	Note 5
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM			VSS		V	
Source Driver							
Source Output Range	Vsout		VAN		VAP	V	
Gamma Reference Voltage(Positive)	VAP		4.45		6.4	V	Note 6
Gamma Reference Voltage(Negative)	VAN		-4.6		-2.65	V	
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2
Output Offset Voltage	VOFFSET				35	mV	Note 3

Basic DC Characteristics

Notes:

1. TA= -30 to 70℃ (to +85℃ no damage).

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

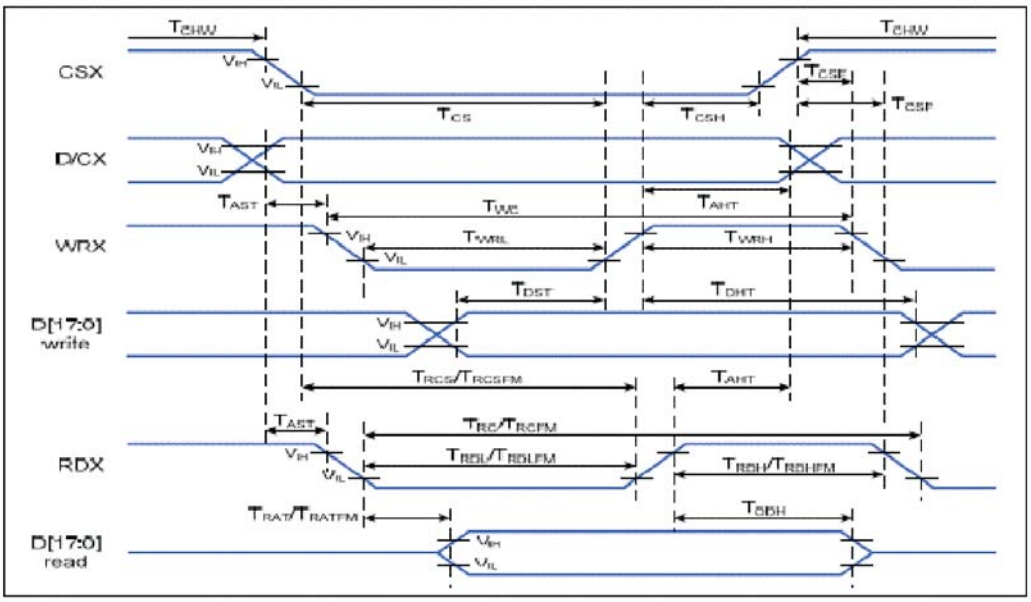
3. The Max. value is between measured point of source output and gamma setting value.

4. When evaluating the maximum and minimum of VGH, VDD=2.8V.

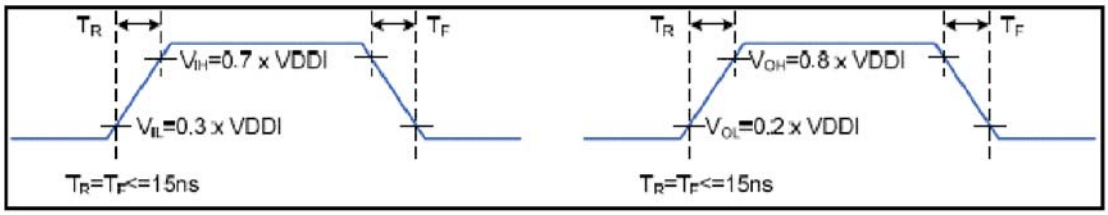
5. The maximum value of |VGH-VGL| can no over 30V.

6. Default register setting of Vcom and Vcomoffset is 20h

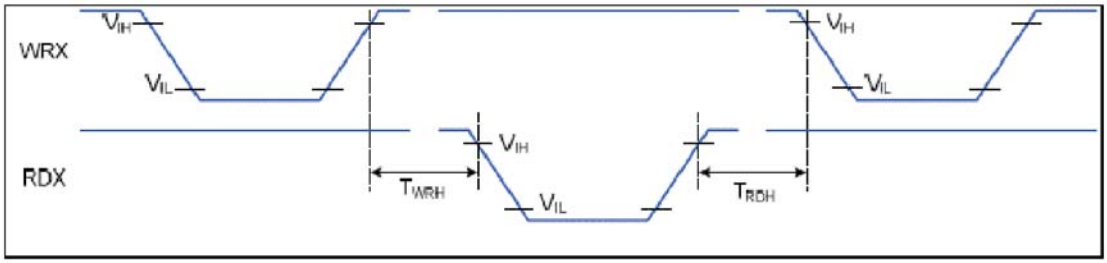
6. 3.Timing



Parallel Interface Timing Characteristics (8080-Series MCU Interface)

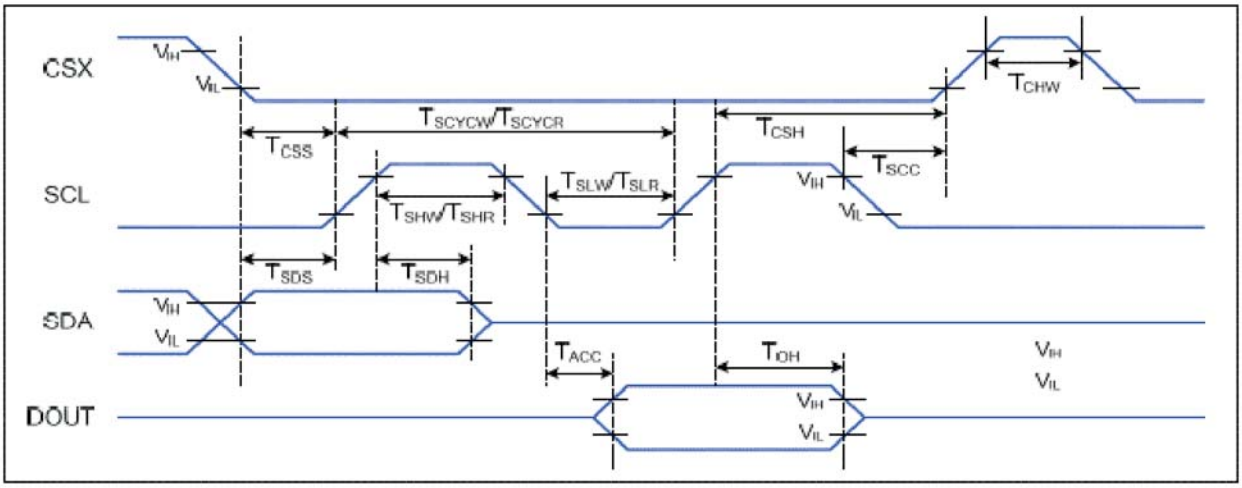


Rising and Falling Timing for I/O Signal

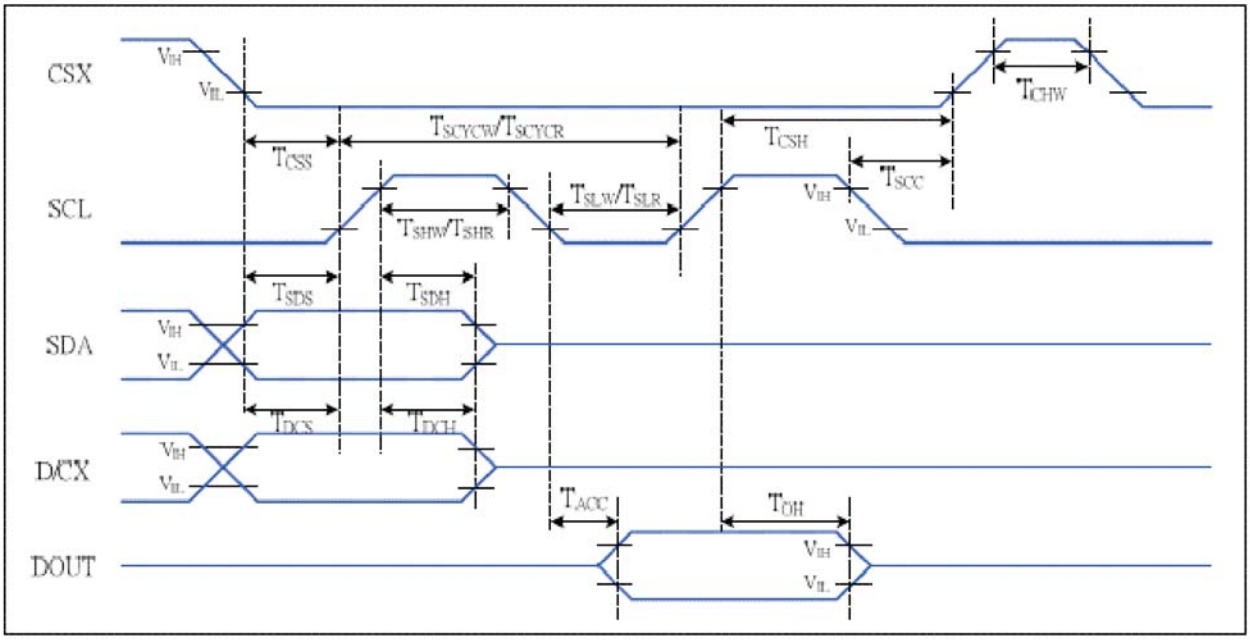


Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.



3-line serial Interface Timing Characteristics



4-line serial Interface Timing Characteristics

6. 4.Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

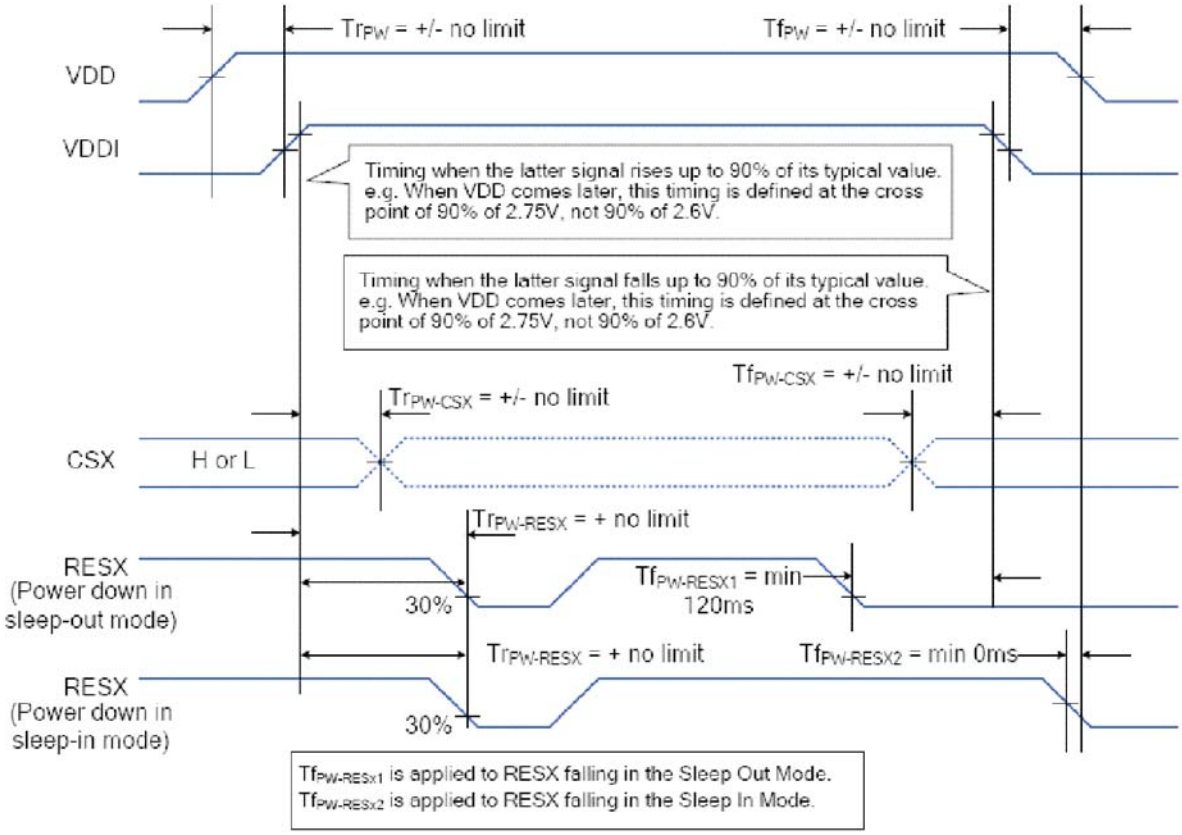
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



7. Optical Characteristics

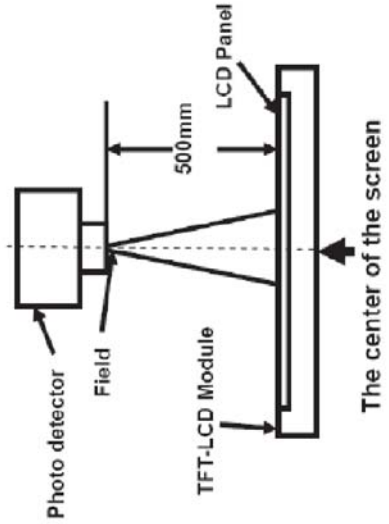
Item		Symbol	Condition	Min	Typ.	Max	Unit	Remark
View Angles		θ T	CR≥10		50		Degree	Note 2
		θ B			20			
		θ L			45			
		θ R			45			
Contrast Ratio		CR	θ = 0°	-	500			Note 1 Note 3
Response Time		$T_{ON}+T_{OFF}$	25° C		16		ms	Note 1 Note 4
Chromaticity	W_x	x		-	0.301	-		Note 1 Note 5
	W_y	y		-	0.337	-		
Uniformity		U		80	85		%	Note 5
Luminance		L		320	350		cd/m^2	Note 1 Note 5

Test Conditions:

1. If=80 mA(Backlight current), VDD =2.8V,the ambient temperature is 25° C.
2. The test systems refer to Note 2.

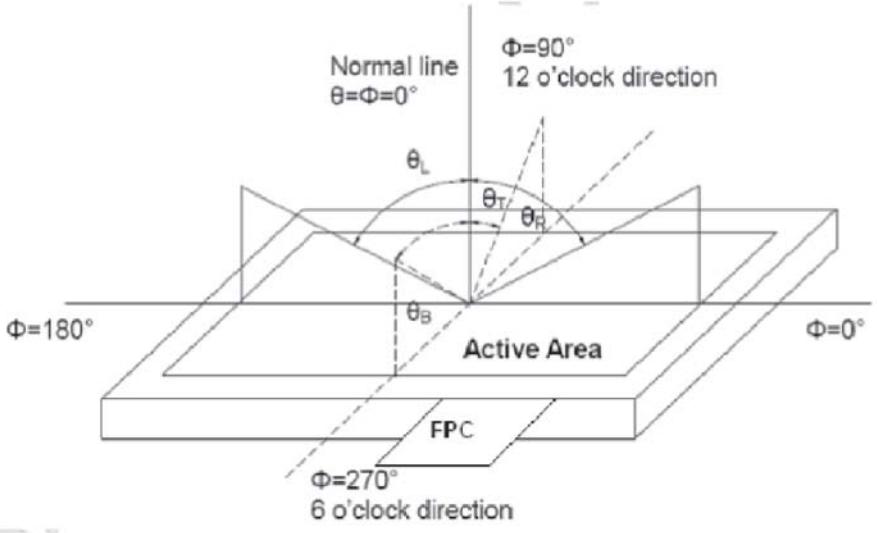
Note1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5Minutes operation, the optical properties are measured at the center point of the LCD screen. ALL input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	CS1000	1°
Luminance		
Lum Uniformity		
Chromaticity	CS1000	
Response Time	DMS703	-

Note2: Definition of viewing angle range and measurement system.
Viewing angle is measured at the center point of the LCD by CONOSCOPE (DMS703)



NOTE3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

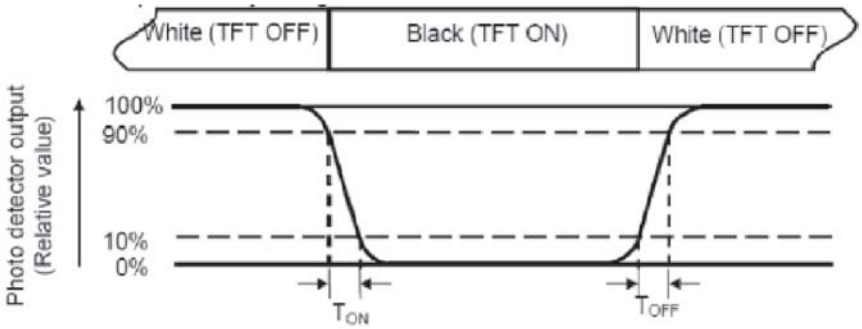
"White state ":The state is that the LCD should drive by Vwhite.

"Black state ":The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined

Note4:Definition of Response time

The response time is defined as the LCD optical switching time interval between "White"state and "Black" state. Rise time (T_{ON})is the time between photo detector output intensity changed from 90% to 10%.And fall time (T_{OFF})is the time between photo detector output intensity changed from 10% to90%.



Note5:Definition of color chromaticity（CIE1931）

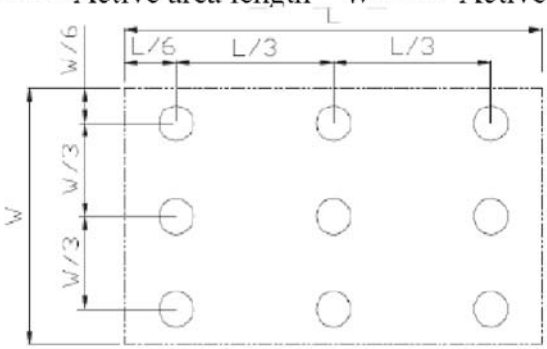
Color coordinates measured at center point of LCD.

Note6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas(Refer Fig.2).Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U)=Lmin/Lmax

L--------Active area length W--------Active area width



L max: The measured Maximum luminance of all measurement position.

L min: The measured Minimum luminance of all measurement position.

Note7: Definition of luminance:

Measure the luminance of white state at center point.

8. Environmental/Reliability Test

No.	Test Item	Test Condition	Inspection after test
1	High Temperature Storage	80±2℃/240 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Sealleak; 3.Non-display; 4.missing segments; 5.Glass crack; 6.Current Idd is twice higher than initial value.
2	Low Temperature Storage	-30±2℃/240 hours	
3	High Temperature Operating	70±2℃/240 hours	
4	Low Temperature Operating	-30±2℃/240 hours	
5	Temperature Cycle	-30℃~ 25℃~ 80℃ × 10cycles (30min.) (5min.) (30min.)	
6	Damp Proof Test	40℃±5℃×90%RH/240 hours	
7	Vibration Test	Frequency：10Hz~55Hz~10Hz Amplitude：1.5mm, X，Y，Z direction for total	
8	Dropping test	Drop to the ground from 1m height, one time, every side of carton. (Packing condition)	
9	ESD test	Voltage:±8KVR: 330Ω C: 150pF Air discharge, 10time	

Remark:
1.The test samples should be applied to only one test item.
2.Sample size for each test item is 5~10pcs.
3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6.Please use automatic switch menu(or roll menu) testing mode when test operating mode.

10. Standard Specifications For Product Quality

10.1. Manner of test:

10.1.1 The test must be under 40W fluorescent light, and the distance of view must be at 30±10cm.

10.1.2 Room temperature 25±5℃ Humidity: (60±10)%RH.

10.2. Quality specification

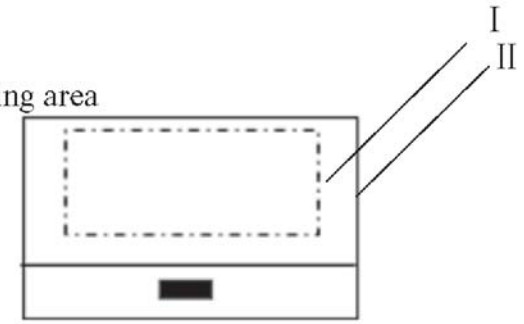
It shall be based on GB2828-87, inspection level Ⅱ .

	IETM	CHECK LEVEL	AQL
MAJOR (MA)	1.Liquid crystal leakage 2.Wrong polarizer 3.Outside dimension 4. Bright dot、Dark dot 5. Display abnormal 6. Class crack	Ⅱ	0.25
MINOR (MI)	1. Spot Defect (Including black spot、white spot、pinhole、foreign particle、bubbles、hurt) 2. fragment 3. Line Defect (Including black line、white line、cratch) 4. Incision defect 5. Newton's ring 6. Other visual defects	Ⅱ	1.0

10.3. Definition of area:

10.3.1 Ⅰ area: viewing area

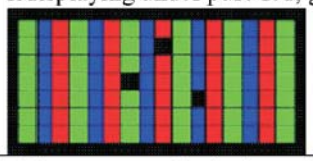
Ⅱ area: outside viewing area



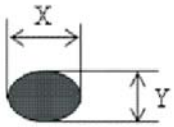
10.4.Standard of appearance test for Ⅰ area: (unit: mm)

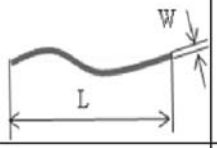
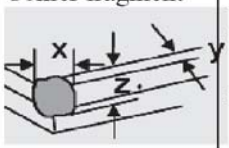
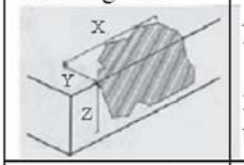
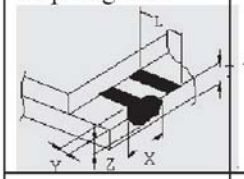
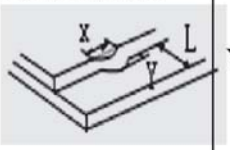
NOTE: Defect ignore for Ⅱ area .

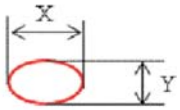
10.4.1 Bright/Dark Dots explain

Name	Explain	Definition
Bright dot	Dots appear bright and unchanged in size in which LCD panel isdisplaying under black pattern	The definition of dot: The size of a defective dot over 1/2 of single pixel dot is regarded as one defective dot . NOTE: One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)
Dark dot	Dots appear dark and unchanged in size in which LCD panel isdisplaying under pure red, green, blue pattern. 	
ADJACENT DOT	Adjacent two sub-pixel are defect（define two dot defect）	

10.4.2 Inspection standard

№	Items	Criterion		Checking Manner	Defect Classes
1	Bright/dark dot	Under 6” (contain 6”)	Bright dot：2 Dark dot：N≤4 **Note:** be more than 5mm apart	Checking with eyes	MAJ
		6”-12”	Bright dot：N≤4 Dark dot：N≤5 Total Bright and Dark Dots：N≤8 **Note ：** 1.Two bright dot defects (red, green, blue, and white) should be larger than 15mm; 2.The distance between black dot defects or black and bright dot defects should be more than 5mm apart.		
2	Spot Defect (Including black spot.white spot. Pinhole.foreign particle.bubbles.hurt）  D=(X+Y)/2	Under 6” （contain 6”）	D≤0.1 Ignore 0.1＜D≤0.35 N≤3 0.35＜D N=0	Checking with eyes	MIN
		6”-12”	D≤0.3 Ignore 0.3＜D≤0.6 N≤4 0.6＜D N=0		

№	Items	Criterion		Checking manner	Defect classes
3	Line Defect (Including black Line.white line. scratch) 	Under 6" (contain 6")	W≤0.02 Ignore 0.02＜W≤0.04 L≤5 N≤2 0.04＜W≤0.06 L≤5 N≤1 W＞0.06 N=0	Checking with eyes	MIN
		6"-12"	W≤0.07 Ignore 0.07＜W≤0.1 L≤10 N≤4 W＞0.1 N=0		
4	Display abnormal	Not allowed		Checking with eyes	MAJ
5	Outside dimension	Accord with drawing		Callipers	MAJ
6	Class crack	Not allowed		Checking with eyes	MAJ
7	Leak	Not allowed		Checking with eyes	MAJ
8	Comer fragment 	X≤3 Y≤3 Z≤T Ignore Note ： 1.No hurt identifying .wire.seal 2.T：Glass thickness X: Length Y: Width Z: thickness		Checking with eyes	MIN
9	Side fragment 	Y≤1 Z≤T Ignore Note ： 1.No hurt identifying .wire.seal 2.T：Glass thickness X: Length Y: Width Z: thickness		Checking with eyes	MIN
	Step fragment 	Y≤1 and Y≤1/4 L		Checking with eyes	MIN
	Incision defect 	Y≤1 and accord with outside dimension		Checking with eyes	MIN

№	Items	Criterion		Checking manner	Defect classes
10	Newton's ring （CTP or Cover board）  D=(X+Y)/2	Under 6" (contain 6") 6"-12"	D≤25 N≤3 D＞25 N=0 D≤70 N≤5 D＞70 N=0	Checking with eyes	MIN